RELIABILITY REPORT

FOR

MAX6476UTxx

PLASTIC ENCAPSULATED DEVICES

January 10, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX6476 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6476 is a low-dropout linear regulator with a fully integrated microprocessor reset circuit. It is available with preset output voltages from +1.5V to +3.3V in 100mV increments and delivers up to 300mA of load current. This device consumes only 82µA of supply current. The low supply current, low dropout voltage, and integrated reset functionality makes this device ideal for battery-powered portable equipment.

The MAX6476 includes a reset output that indicates when the regulator output drops below standard microprocessor supply tolerances (-7.5% or -12.5% of nominal output voltage). This eliminates the need for an external microprocessor supervisor, while ensuring that supply voltages and clock oscillators have stabilized before processor activity is enabled. Push-pull and open-drain active-low reset outputs are available, with reset timeout periods of 2.5ms, 20ms, 150ms, or 1200ms (min).

The MAX6476 also has a shutdown feature that reduces the supply current to 0.1µA (typ). The MAX6476 features a remote feedback sense pin for use with an external NPN transistor for higher-current applications. The MAX6476 is available in a 6-pin SOT23 All devices are specified for operation from -40°C to +85°C.

B. Absolute Maximum Ratings

Item	Rating
(All voltages referenced to GND, unless otherwise noted.)	
IN, /SHDN , OUT, FB	-0.3V to +7V
/MR , SET	-0.3V to (V_{IN} + 0.3V)
/RESET (push-pull)	-0.3V to (V_{OUT} + 0.3V)
/RESET (open drain)	-0.3V to +7V
OUT Short Circuit	Continuous
Input/Output Current (all pins except IN and OUT)	20mA
Continuous Power Dissipation (TA = +70°C)	
6-Pin SOT23	727Mw
Derates above +70°C	
6-Pin SOT23	9.1mW/°C
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function: 300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

B. Process: S8 (Standard 0.8 micron silicon gate CMOS)

C. Number of Device Transistors: 1041

D. Fabrication Location: California, USA

E. Assembly Location: Malaysia

F. Date of Initial Production: July, 2002

III. Packaging Information

A. Package Type: **6-Pin SOT23 Flip-Chip**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: n/A

E. Bondwire: 6 mil dia. Bump

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-1601-0202

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 85 x 45 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 0.8 microns (as drawn)

F. Minimum Metal Spacing: 0.8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

B.

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 45 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 24.13 \times 10^{-9}$

$\lambda = 24.13$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6058) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The MS78-7 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX6476UTxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

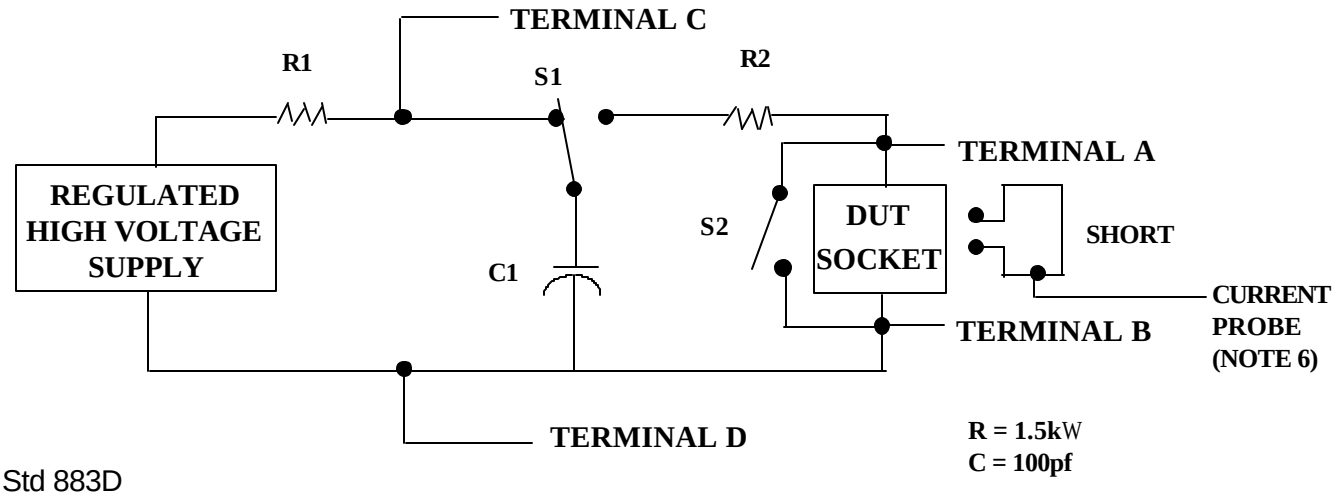
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

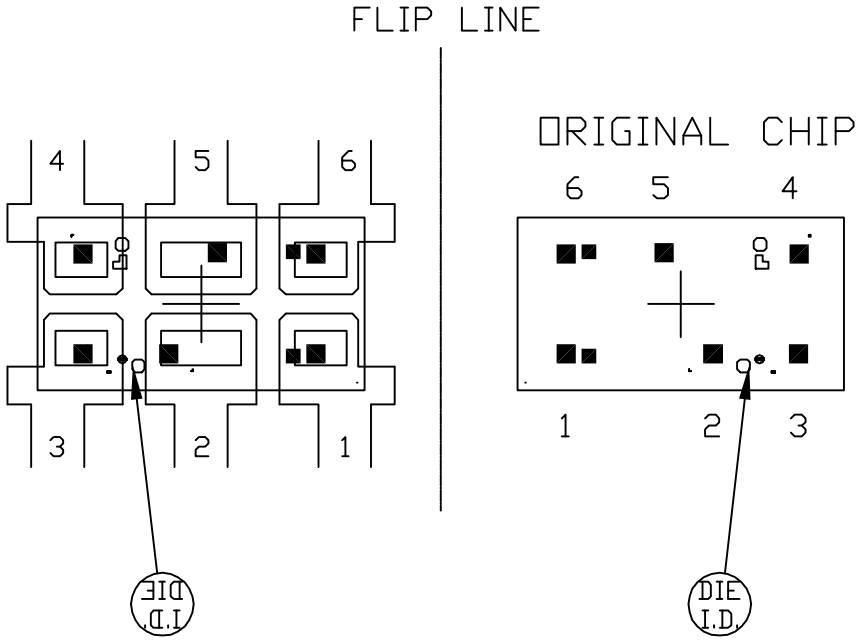
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

FLIP CHIP PKG.



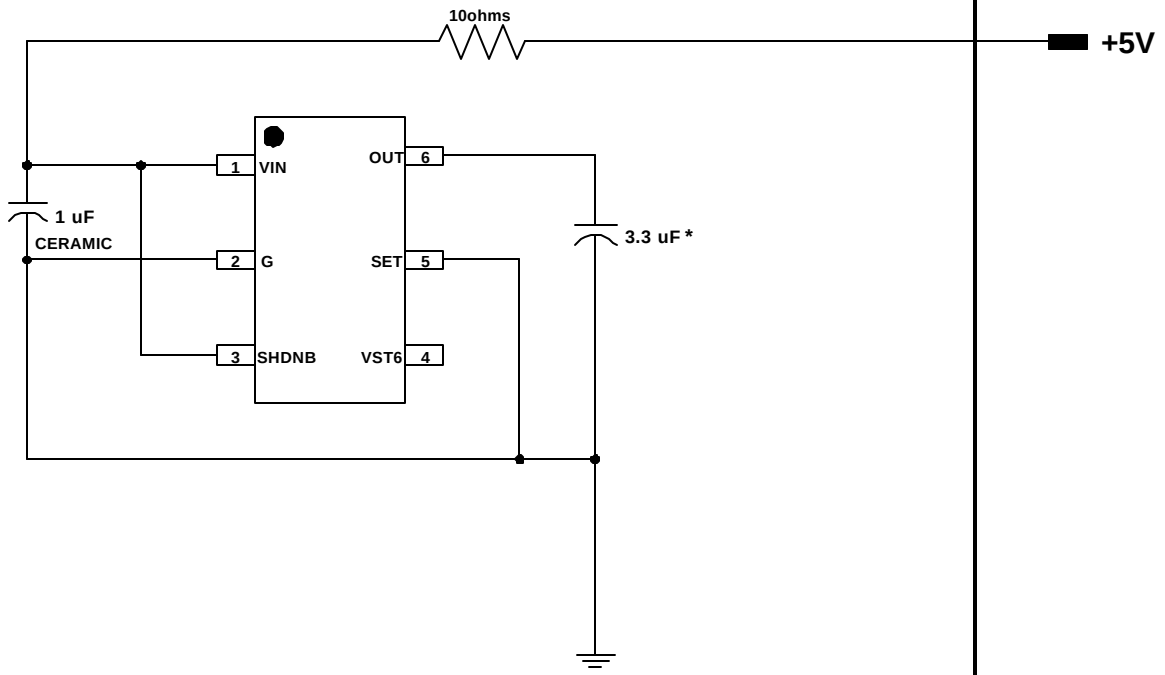
PAD 2 OUT OF BOUND WINDOW BY -.0038 IN X-DIRECTION
WAIVED BY PACKAGING ENGINEERING.

NOTE: CAVITY DOWN

PKG. CODE: U6F-6		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: FLIP CHIP	PKG.			BOND DIAGRAM #: 05-1601-0202	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX6470 (MS78Z)
PACKAGE: 6 - SOT
MAX. EXPECTED CURRENT = 300 uA

DRAWN BY: TEK TAN

NOTES: * 3.3 uF must be low ESR (0.02 to 0.2 ohm) ceramic. Use 7R cap (high temp). Keep trace from pin #6 short.