

RELIABILITY REPORT  
FOR  
**MAX4524xxB**  
PLASTIC ENCAPSULATED DEVICES

August 29, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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## Conclusion

The MAX4524 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX4524 is a low-voltage, single-supply CMOS analog switch configured as a 4-channel multiplexer/demultiplexer with an inhibit input to simultaneously open all signal paths.

This devices operate from a single supply of +2V to +12V and is optimized for operation with +3V or +5V supplies. On-resistance is 200 $\Omega$  with a +5V supply and 500 $\Omega$  with a +3V supply. The switch can handle Rail-to-Rail® analog signals. The off-leakage current is only 2nA at +25°C or 20nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
(Voltages Referenced to GND)	
V+	-0.3V, +13V
Voltage into any terminal (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current into any Terminal	$\pm$ 20mA
Peak Current, NO, NC or COM_ (pulsed at 1ms,10% duty cycle)	$\pm$ 40mA
Operating Temperature Ranges	
MAX4524Cxx	0°C to +70°C
MAX4524Exx	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Continuous Power Dissipation (TA = +70°C)	
10-Lead $\mu$ MAX	330mW
10-Lead Thin DFN	1951mW
Derates above +70°C	
10-Lead $\mu$ MAX	4.1mW/°C
10-Lead Thin DFN	24.4mW/°C

**Note 1:** Voltages exceeding V+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

## II. Manufacturing Information

A. Description/Function:	Low-Voltage, Single-Supply Multiplexer and Switch
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	219
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Philippines or Thailand
F. Date of Initial Production:	January, 1998

## III. Packaging Information

A. Package Type:	<b>10-Lead uMAX</b>	<b>10-Lead Thin DFN (3 X 3)</b>
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0042	# 05-9000-0667
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1

## IV. Die Information

A. Dimensions:	53 x 69 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Executive Director)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.57 \times 10^{-9}$$

$$\lambda = 13.57 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5325) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The AH14-3 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX4524xxB**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX	77	0
			QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

## Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

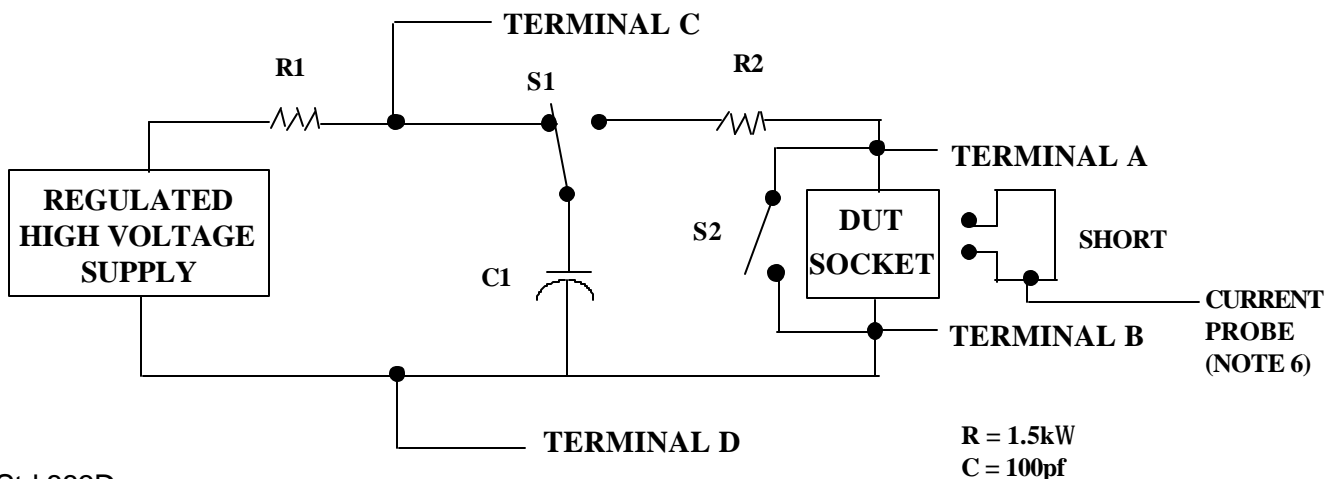
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

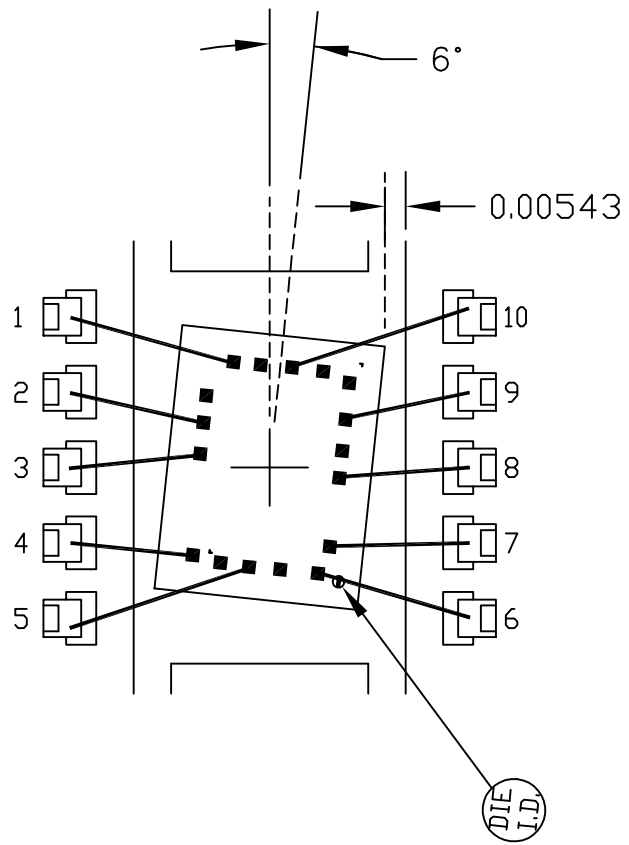
### 3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

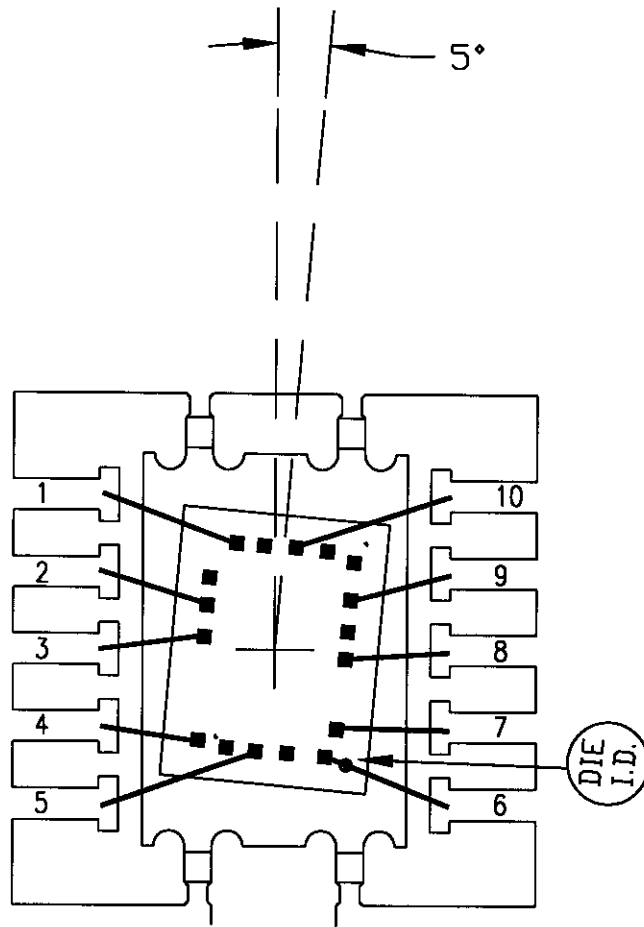


3x3x0.8 MM QFN THIN PKG.

EXPOSED PAD PKG.



PKG. CODE: T1033-1		SIGNATURES	DATE	<b>MAXIM</b> CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 71x102	PKG. DESIGN			BOND DIAGRAM #: 05-9000-0667	REV: A



PKG.CODE: U10-2

CAV./PAD SIZE:  
68X94

APPROVALS

DATE

**MAXIM**

BUILDSHEET NUMBER:  
05-1201-0042

REV:  
A

PKG.  
DESIGN



