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RELIABILITY REPORT

FOR

MAX44268EWL+T

WAFER LEVEL PRODUCTS

April 25, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

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Conclusion

The MAX44268EWL+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX44268 is an ultra-small and low-power dual comparator ideal for battery-powered applications such as cell phones, notebooks, and portable medical devices that have extremely aggressive board space and power constraints. The comparator is available in a miniature 1.3mm x 1.3mm, 9-bump WLP package, making it the industryâ€™s smallest dual comparator. The IC can be powered from supply rails as low as 1.8V and up to 5.5V. It also features a 1.236V ±1% reference and a 0.7µA typical supply current per comparator. It has a rail-to-rail input structure and a unique output stage that limits supply current surges while switching. This design also minimizes overall power consumption under dynamic conditions. The IC has open-drain outputs, making it suitable for mixed voltage systems. The IC also features internal filtering to provide high RF immunity. It operates over a -40°C to +85°C temperature.

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II. Manufacturing Information

A. Description/Function:	1.3mm x 1.3mm, Low-Power Dual Comparator with Reference
B. Process:	B8
C. Number of Device Transistors:	180
D. Fabrication Location:	California or Texas
E. Assembly Location:	Japan or Texas
F. Date of Initial Production:	December 20, 2011

III. Packaging Information

A. Package Type:	9 bmp WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A (mil dia.)
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-4559
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	84°C/W
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	51 X 51 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.04 @ 25C and 0.73 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot J2MYAQ001C, D/C 1147)

The CM95-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX44268EWL+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	J2MSAQ001B, D/C 1122

Note 1: Life Test Data may represent plastic DIP qualification lots.

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