MAX2268EUE
Rev. A

RELIABILITY REPORT

FOR

MAX2268EUE

PLASTIC ENCAPSULATED DEVICES

February 14, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX2268 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX2268 power amplifier ia optimized for IS-98-based CDMA and PDC cellular telephones operating in the Japanese cellular-frequency band. When matched for CDMA operation, the amplifiers achieve 27dBm output power with 35% efficiency (MAX2268), with margin over the adjacent and alternate channel specification. At a +17dBm output-a very common power level for CDMA phones-the MAX2268 still has 7% efficiency, yielding excellent overall talk time.

The MAX2268 has internally referenced bias ports that are normally terminated with simple resistors. The bias ports allow customization of ACPR margin and gain. They can also be used to "throttle back" bias current when generating low power levels. The MAX2268 hasexcellent gain stability over temperature (±0.8dB), so over-design of driver stages and excess driver current are dramatically reduced, further increasing the phone's talk time. The devices can be operated from +2.7V to +4.5V while meeting all ACPR specifications over the entire temperature range.

The devices is packaged in a 16-pin TSSOP with exposed paddle (EP).

B. Absolute Maximum Ratings

Item	Rating
VCC to GND (no RF input)	-0.3V to +5V
Logic Inputs to GND	-0.3V to (VCC + 0.3V)
BIAS_ _ to GND	-0.3V to (VCC + 0.3V)
RF Input Power	+6dBm (20mW)
Logic Input Current	±10mA
Output VSWR with +6dBm Input	2.5:1
Total DC Power Dissipation (TPADDLE = +100°C)	
16-Pin TSSOP-EP (derate 60mW/°Cabove TPADDLE = +100°C)	4W
Theta JA	8°C/W
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°CV_{CC} to GND

II. Manufacturing Information

A. Description/Function: +2.7V, Single-Supply, Cellular-Band Linear Power Amplifiers

B. Process: GST2 – High Speed Double Poly-Silicon Bipolar Process

C. Number of Device Transistors: 1256

D. Fabrication Location: Oregon, USA

E. Assembly Location: Korea

F. Date of Initial Production: October, 1999

III. Packaging Information

A. Package Type: **16-Pin TSSOP-EP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.2 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-2201-0024

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 68 x 62 mils

B. Passivation: Si3N4/SiO2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Poly / Au

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)

F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 50 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 9.70 \times 10^{-9}$

λ = 9.70 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-B2A**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The WR45-3 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA.

Table 1
Reliability Evaluation Test Results

MAX2268EUE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		50	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

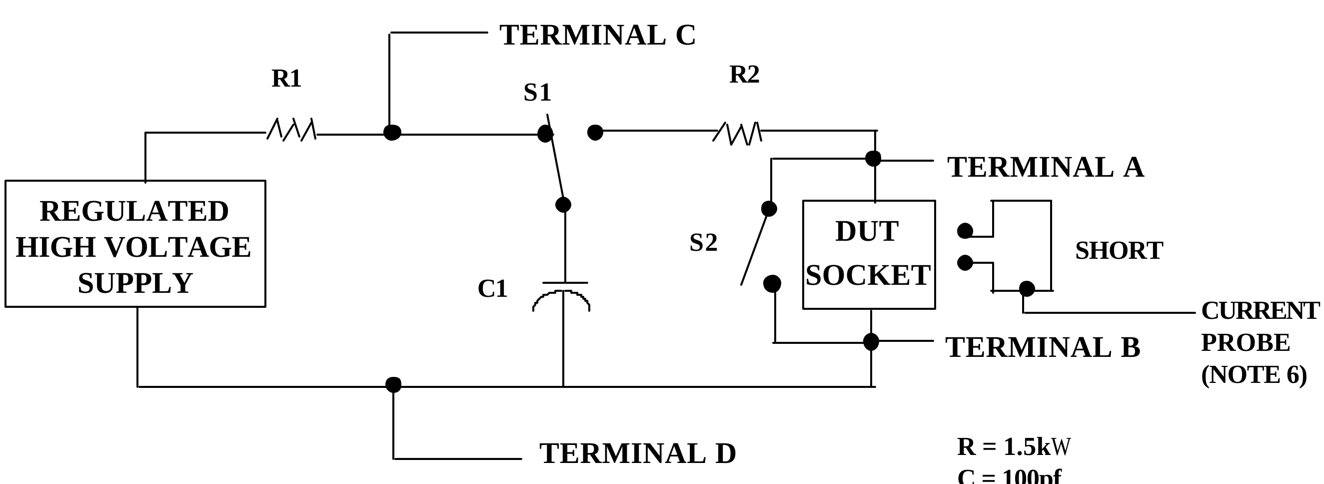
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

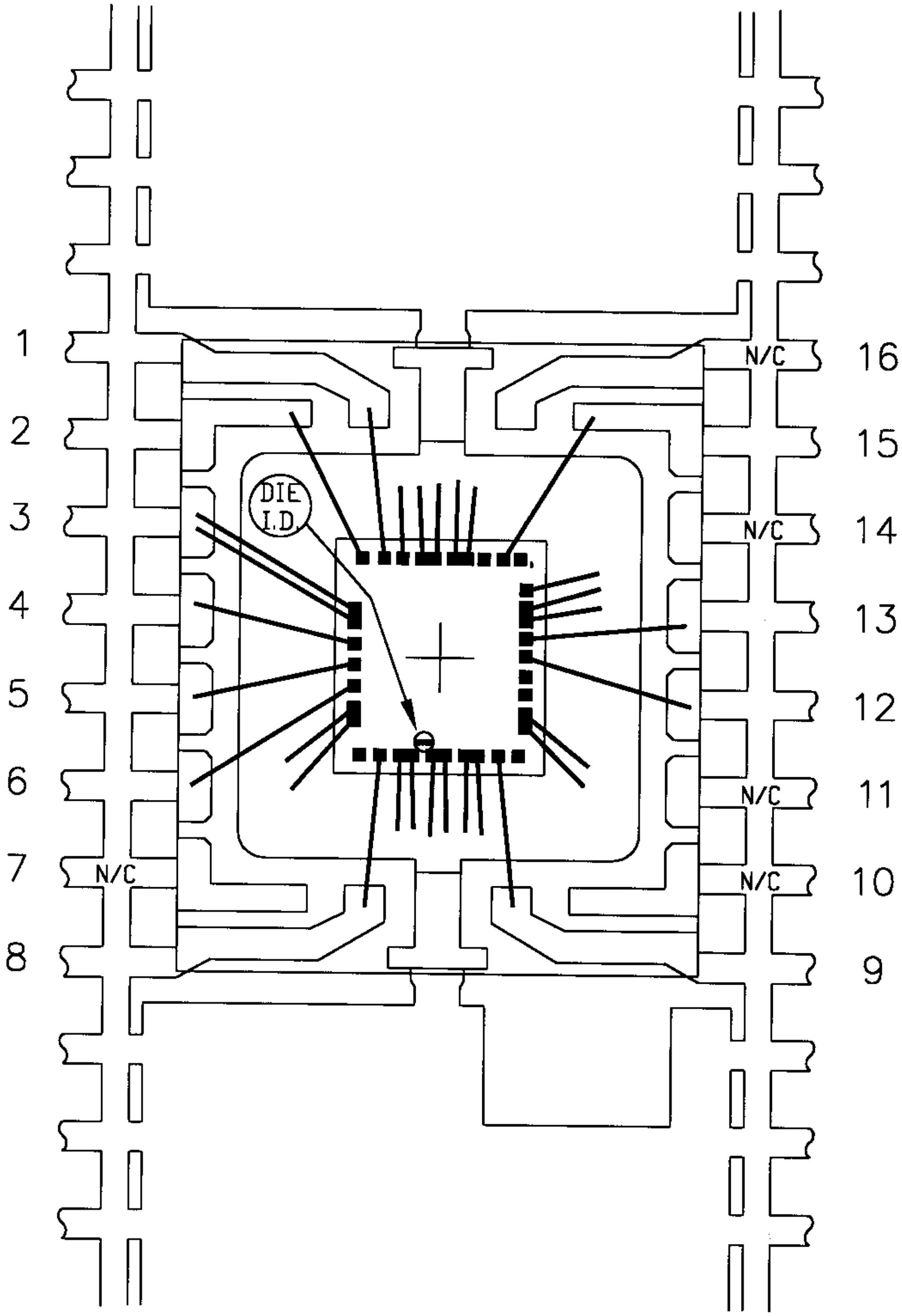
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





MAX 2265
MAX 2268

SPECIAL INSTRUCTIONS:
8 MIL THICK DIE, 15 MIL MAX DOWN BOND WIRES,
6 MIL LOOP HT.

PKG.CODE: U16E-3		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 118x118	PKG. DESIGN			BUILDSHEET NUMBER: 05-2201-0024 REV.: B