

RELIABILITY REPORT
FOR
MAX1836ExTxx
PLASTIC ENCAPSULATED DEVICES

August 3, 2006

MAXIM INTEGRATED PRODUCTS

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Written by

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Quality Assurance
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Conclusion

The MAX1836 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1836 high-efficiency step-down converter provides a preset 3.3V or 5V output voltage from supply voltages as high as 24V. Using external feedback resistors, the output voltage may be adjusted from 1.25V to V_{IN} . An internal current-limited switching MOSFET delivers load currents up to 125mA (MAX1836) or 250mA (MAX1837).

The unique current-limited control scheme, operating with duty cycles up to 100%, minimizes the dropout voltage (120mV at 100mA). Additionally, this control scheme reduces supply current under light loads to 12 μ A. High switching frequencies allow the use of tiny surface-mount inductors and output capacitors.

The MAX1836 step-down converter with internal switching MOSFETs is available in a 6-pin SOT23 package, making it ideal for low-cost, low-power, space-sensitive applications. For increased output drive capability, use the MAX1776 step-down converter that uses an internal 24V switch to deliver up to 500mA. For even higher currents, use the MAX1626/ MAX1627 step-down controllers that drive an external P-channel MOSFET to deliver up to 20W.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN, SHDN to GND	-0.3V to +25V
LX to GND	-2V to ($V_{IN} + 0.3V$)
OUT, FB to GND	-0.3V to +6V
Continuous Power Dissipation ($T_A = +70^{\circ}C$) (Note 1)	
6-Pin SOT23 (derate 8.7mW/ $^{\circ}C$ above +70 $^{\circ}C$)	696mW
6-Pin TDFN (derate 24.4mW/ $^{\circ}C$ above +70 $^{\circ}C$)	1951mW
Operating Temperature Range	-40 $^{\circ}C$ to +85 $^{\circ}C$
Junction Temperature	+150 $^{\circ}C$
Storage Temperature Range	-65 $^{\circ}C$ to +150 $^{\circ}C$
Lead Temperature (soldering, 10s)	+300 $^{\circ}C$

Note 1: Thermal properties are specified with product mounted on PC board with 1in2 of copper area and still air.

II. Manufacturing Information

A. Description/Function:	24V Internal Switch, 100% Duty Cycle, Step-Down Converters
B. Process:	B8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors:	731
D. Fabrication Location:	Texas or California, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	January, 2001

III. Packaging Information

A. Package Type:	6-Pin TDFN-EP	6-Pin SOT23-6
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin	Solder Plate or 100% Matte Tin
D. Die Attach:	Nonconductive Epoxy	Nonconductive Epoxy
E. Bondwire:	Gold (1 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-1489	# 05-9000-2152
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions:	45 x 90 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 79 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

△ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.92 \times 10^{-9}$$

$$\lambda = 13.92 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-5648) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.17 @ 25°C and 2.92 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PY36 die type has been found to have all pins able to withstand a transient pulse of $\pm 1000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX1836ExTxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		79	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TDFN	77	0
			SOT	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

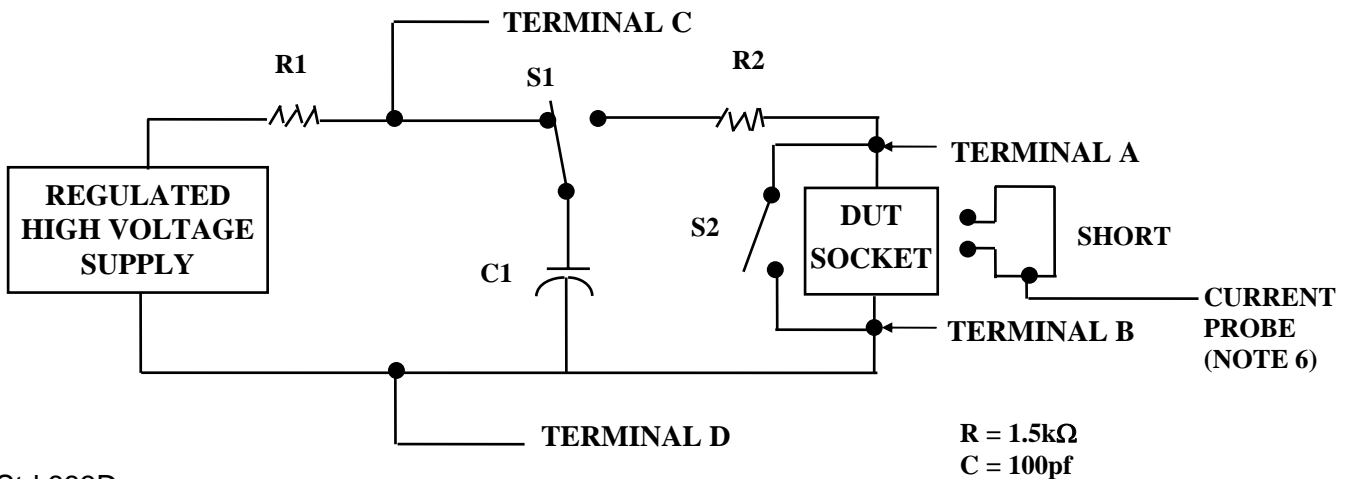
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

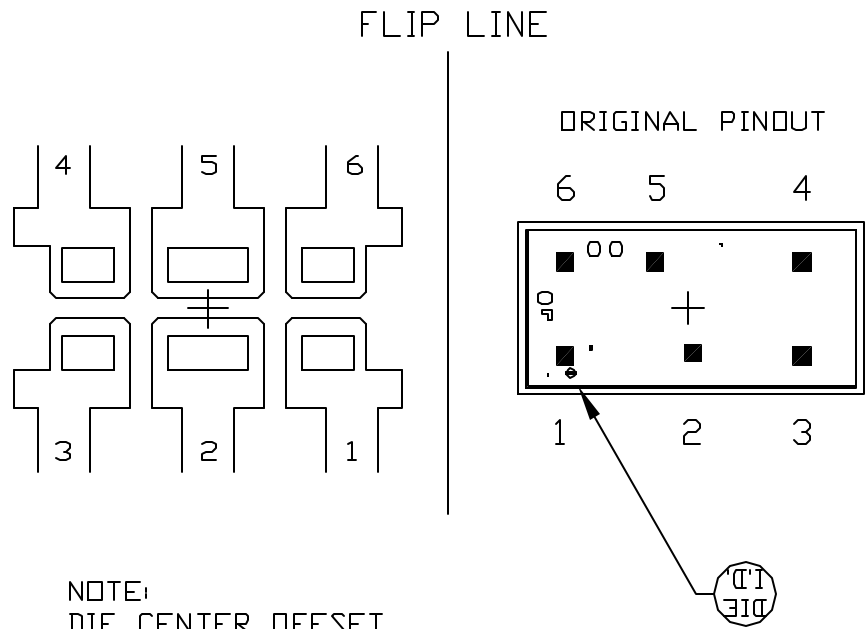
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



FLIP CHIP PKG.
w/HIGH LEAD BUMP,
MATTE TIN PLATE.



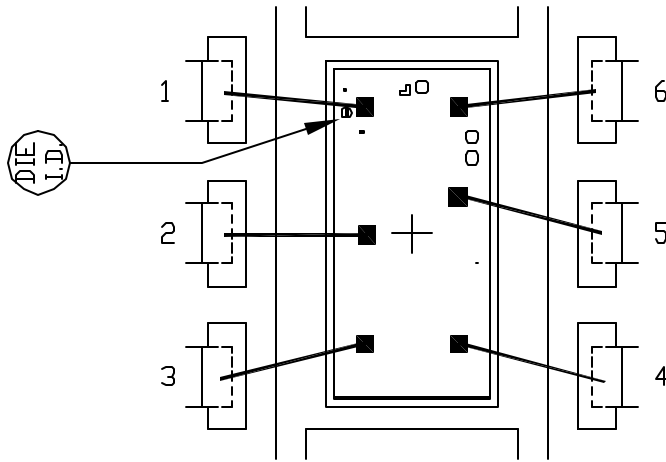
NOTE:
DIE CENTER OFFSET
1 MIL TO THE LEFT.

NOTE: CAVITY DOWN

PKG. CODE: U6FH-6		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: FLIP CHIP	PKG. DESIGN			BOND DIAGRAM #: 05-9000-2152
				REV: A

3x3x0.8 MM TDFN PKG.

EXPOSED PAD PKG.



PKG. CODE: T633-1

SIGNATURES

DATE

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CAV./PAD SIZE:
71x102

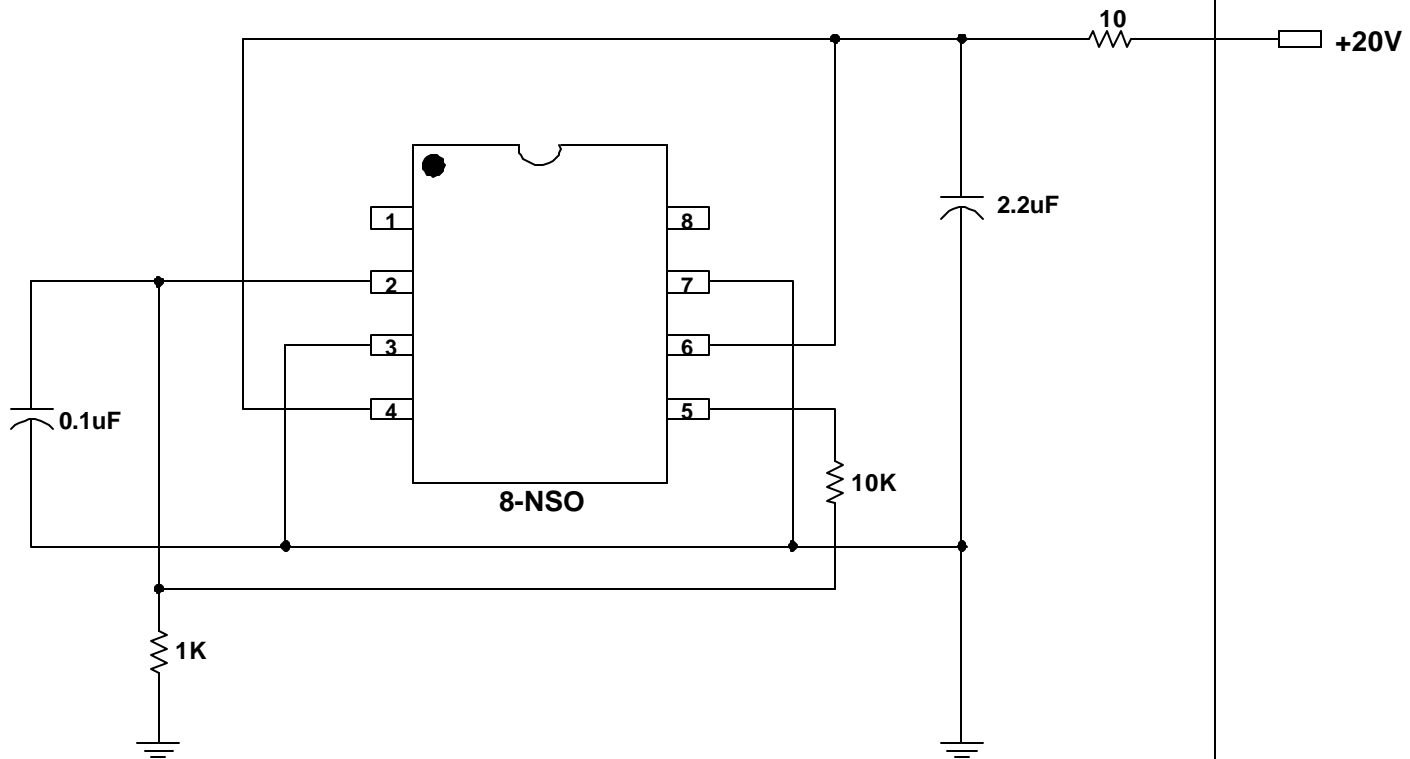
PKG.
DESIGN

BOND DIAGRAM #:
05-9000-1489

REV:
A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 1836/1837

MAX. EXPECTED CURRENT = 3mA