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RELIABILITY REPORT

FOR

MAX17604ATA+T

PLASTIC ENCAPSULATED DEVICES

December 16, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

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Conclusion

The MAX17604ATA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. ....Device Description
II. ....Manufacturing Information
III. ....Packaging Information
.....Attachments
IV. ....Die Information
V. ....Quality Assurance Information
VI. ....Reliability Evaluation

I. Device Description

A. General

The MAX17600-MAX17605 devices are high-speed MOSFET drivers capable of sinking /sourcing 4A peak currents. The devices have various inverting and noninverting part options that provide greater flexibility in controlling the MOSFET. The devices have internal logic circuitry that prevents shoot-through during output-state changes. The logic inputs are protected against voltage spikes up to +14V, regardless of VDD voltage. Propagation delay time is minimized and matched between the dual channels. The devices have very fast switching time, combined with short propagation delays (12ns typ), making them ideal for high-frequency circuits. The devices operate from a +4V to +14V single power supply and typically consume 1mA of supply current. The MAX17600/MAX17601 have standard TTL input logic levels, while the MAX17603 /MAX17604/MAX17605 have CMOS-like high-noise margin (HNM) input logic levels. The MAX17600/MAX17603 are dual inverting input drivers, the MAX17601/MAX17604 are dual noninverting input drivers, and the MAX17602/MAX17605 devices have one noninverting and one inverting input. These devices are provided with enable pins (ENA, ENB) for better control of driver operation.   These devices are available in 8-pin (3mm x 3mm) TDFN, 8-pin (3mm x 5mm) µMAX®, and 8-pin SO packages and operate over the -40°C to +125°C temperature range.

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II. Manufacturing Information

A. Description/Function:	4A Sink/Source Current, 12ns, Dual MOSFET Drivers
B. Process:	S18
C. Number of Device Transistors:	480
D. Fabrication Location:	California
E. Assembly Location:	Taiwan, China, Thailand
F. Date of Initial Production:	December 22, 2011

III. Packaging Information

A. Package Type:	8L-TDFN-CU
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4732
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8°C/W

IV. Die Information

A. Dimensions:	46.85X57.87 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot S24Y0Q001B, D/C 1138)

The PI19-4 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX17604ATA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	S24YXQ001F, 1208

Note 1: Life Test Data may represent plastic DIP qualification lots.

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