RELIABILITY REPORT
FOR
MAX17506ATP+T
PLASTIC ENCAPSULATED DEVICES

July 04, 2015

MAXIM INTEGRATED
160 RIO ROBLES
SAN JOSE, CA 95134

Approved by

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<th>Eric Wright</th>
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<tr>
<td>Quality Assurance</td>
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<tr>
<td>Reliability Engineering</td>
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Conclusion

The MAX17506ATP+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. ........Device Description   IV. .......Die Information
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I. Device Description

A. General

The MAX17506 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated high-side MOSFET operates over a 4.5V to 60V input. The converter can deliver up to 5A and generates output voltages from 0.9V up to 0.9 x VIN. The feedback (FB) voltage is accurate to within ±1.4% over -40°C to 125°C. The MAX17506 uses peak current-mode control. The device can be operated in the pulse-width modulation (PWM), pulse-frequency modulation (PFM), and discontinuous conduction mode (DCM) control schemes. The device is available in a 20-pin (5mm x 5mm) Thin QFN (TQFN) package. Simulation models are available.
II. Manufacturing Information

A. Description/Function: 4.5V-60V, 5A, High-Efficiency, Synchronous Step-Down DC-DC Converter with Internal Compensation

B. Process: S18

C. Number of Device Transistors: 30533

D. Fabrication Location: USA

E. Assembly Location: Taiwan, Thailand

F. Date of Initial Production: December 17, 2014

III. Packaging Information

A. Package Type: 20-pin TQFN

B. Lead Frame: Copper

C. Lead Finish: 100% Matte Tin

D. Die Attach: Conductive

E. Bondwire: Cu (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: #05-9000-5652

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1

J. Single Layer Theta Ja: 48°C/W

K. Single Layer Theta Jc: 2°C/W

L. Multi Layer Theta Ja: 30°C/W

M. Multi Layer Theta Jc: 2°C/W

IV. Die Information

A. Dimensions: 119.2913 X 107.0866 mils

B. Passivation: Si3N4/SiO2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier

D. Backside Metallization: None

E. Minimum Metal Width: 0.23 microns (as drawn)

F. Minimum Metal Spacing: 0.23 microns (as drawn)

G. Bondpad Dimensions: None

H. Isolation Dielectric: SiO2

I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:
   Don Lipps (Manager, Reliability Engineering)
   Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level:
   0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate:
   < 50 ppm

D. Sampling Plan:
   Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

   \[ \lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \]  
   \[ \text{(Chi square value for MTTF upper limit)} \]

   (where $4340 =$ Temperature Acceleration factor assuming an activation energy of 0.8eV)

   \[ \lambda = 13.7 \times 10^{-9} \]

   \[ \lambda = 13.7 \text{ F.I.T.} \text{ (60% confidence level @ 25°C)} \]

   The following failure rate represents data collected from Maxim Integrated’s reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

   The PI03-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.
### Table 1
Reliability Evaluation Test Results

**MAX17506ATP+T**

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test</td>
<td>(Note 1)</td>
<td>DC Parameters &amp; functionality</td>
<td>80</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ta = 135°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
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<td></td>
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<tr>
<td></td>
<td>Time = 192 hrs.</td>
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Note 1: Life Test Data may represent plastic DIP qualification lots.