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RELIABILITY REPORT

FOR

MAX14761ETB+T

PLASTIC ENCAPSULATED DEVICES

May 15, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineering

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Conclusion

The MAX14761ETB+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14759/MAX14761/MAX14763 analog switches are capable of passing bipolar signals that are beyond their supply rails. These devices operate from a single +3.0V to +5.5V supply and support signals in the -25V to +25V range. The MAX14759 is a single-pole/single-throw (SPST) analog switch, while the MAX14761 is a dual-SPST analog switch. The MAX14763 is a single-pole/double-throw (SPDT) analog switch. The MAX14759 features 1 (max) on-resistance with a ±200nA (max) on-leakage current. The MAX14761/MAX14763 feature 2 (max) on-resistance with a ±100nA (max) on-leakage current. The low on-resistance and high bandwidth allow use in digital- and analog-signal switching applications. The MAX14759/MAX14763 is available in an 8-pin (3mm x 3mm) TDFN package. The MAX14761 is available in a 10-pin (3mm x 3mm) TDFN package. These devices are specified over the -40°C to +85°C extended temperature range.

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II. Manufacturing Information

A. Description/Function:	Above- and Below-the-Rails Low On-Resistance Analog Switches
B. Process:	S18
C. Number of Device Transistors:	2840
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan, Thailand
F. Date of Initial Production:	September 23, 2011

III. Packaging Information

A. Package Type:	10-pin TDFN-CU
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Cu (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5581
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	9°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	9°C/W

IV. Die Information

A. Dimensions:	62.9921 X 93.7008 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AK09-2 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1

Reliability Evaluation Test Results

MAX14761ETB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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