



RELIABILITY REPORT
FOR
MAX13042EETD+
PLASTIC ENCAPSULATED DEVICES

April 8, 2010

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX13042EETD+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX13042E-MAX13045E 4-channel, bidirectional level translators provide the level shifting necessary for 100Mbps data transfer in multivoltage systems. The MAX13042E-MAX13045E are ideally suited for level translation in systems with four channels. Externally applied voltages, VCC and VL, set the logic levels on either side of the device. Logic signals present on the VL side of the device appear as a high-voltage logic signal on the VCC side of the device and vice-versa. The MAX13042E-MAX13045E operate at full speed with external drivers that source as little as 4mA output current or larger. Each input/output (I/O) channel is pulled up to VCC or VL by an internal 30 μ A current source, allowing the MAX13042E-MAX13045E to be driven by either push-pull or open-drain drivers. The MAX13042E-MAX13045E feature an enable (EN) input that places the devices into a low-power shutdown mode when driven low. The MAX13042E-MAX13045E feature an automatic shutdown mode that disables the part when VCC is less than V L. The state of I/O VCC_ and I/O VL_ during shutdown is chosen by selecting the appropriate part version. (See the *Ordering Information/Selector Guide* in the full data sheet). The MAX13042E-MAX13045E operate with VCC voltages from +2.2V to +3.6V and VL voltages from +1.62V to +3.2V, making them ideal for data transfer between low-voltage ASIC/PLDs and higher voltage systems. The MAX13042E-MAX13045E are available in 12-bump UCSP(tm) (1.54mm x 2.12mm) and 14-pin TDFN (3mm x 3mm) packages, and operate over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	1.62V to 3.6V Improved High-Speed LLT
B. Process:	S4
C. Number of Device Transistors:	
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Thailand
F. Date of Initial Production:	April 11, 2007

III. Packaging Information

A. Package Type:	14-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2696
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8.3°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8.3°C/W

IV. Die Information

A. Dimensions:	87 X 64 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$
$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.05 @ 25C and 0.83 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The LT09 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX13042EETD+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data