RELIABILITY REPORT FOR

MAX98925EWV+T

WAFER LEVEL DEVICES

May 7, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX98925EWV+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX98925 is a high-efficiency mono Class DG audio amplifier featuring an integrated boost converter and ADCs for sensing speaker current, speaker voltage, and battery supply voltage. The boost converter output voltage is programmable from 6.5V to 8.5V in 0.25V increments from a battery voltage as low as 2.5V. The boosted supply efficiently delivers up to 6.5W at 10% THD+N into a 4Ω load. The boost switching frequency of 2.3MHz allows a small case size 1µH external inductor to be used. The Class DG multilevel amplifier can be supplied externally, bypassing the boost converter and removing the need for an external inductor. With an 8.5V external sup- ply, the IC is up to 87% efficient outputting 3.5W into an 8Ω load. The MAX98925 digital audio interface (DAI) supports I2S, left-justified, and 8-channel TDM formats and can act as master or slave. Either BCLK or MCLK can be used as the internal clock source providing system level flexibility. The speaker current and voltage sense ADCs have 16- bit resolution. Speaker current/voltage sense and bat- tery/boost sense are output from the DAI at the sample rate defined by LRCLK. Battery and boost supply data can also be read from the I2C interface. Active emissions limiting edge rate and overshoot control circuitry, together with Class DG multilevel modulation, minimize EMI and eliminate the need for output filtering found in traditional Class D devices. Automatic level control (ALC) reduces amplifier gain as the battery voltage drops to prevent system reset due to battery collapse. Threshold, maximum attenuation, and attack/release rates are programmable. The IC is available in a 0.5mm pitch 30-bump WLP pack- age. It is specified over the extended, -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	8.5V Boosted Class DG Speaker Amplifier with I/V Sense
B. Process:	S18
C. Number of Device Transistors:	430761
D. Fabrication Location:	Taiwan
E. Assembly Location:	Taiwan
F. Date of Initial Production:	June 28, 2014

III. Packaging Information

A. Package Type:	30-bump WLP 5x6
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-5740
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	119.685 X 127.559 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot VAQP3Q003A D/C 1401)

The AX98-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114
ESD-CDM: +/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX98925EWV+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	CAQP3Q001B, D/C 1350

Note 1: Life Test Data may represent plastic DIP qualification lots.