RELIABILITY REPORT

FOR

MAX9775EBX

CHIP SCALE DEVICES

September 29, 2007

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by

Ken Wendel
Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX9775 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9775/MAX9776 combine a high-efficiency Class D, stereo/mono audio power amplifier with a mono DirectDrive™ receiver amplifier and a stereo DirectDrive headphone amplifier.

Maxim's 3rd-generation, ultra-low-EMI, Class D audio power amplifiers provide Class AB performance with Class D efficiency. The MAX9775/MAX9776 deliver 1.5W per channel into a 4Ω load from a 5V supply and offer efficiencies up to 79%. Active emissions limiting circuitry and spread-spectrum modulation greatly reduce EMI, eliminating the need for output filtering found in traditional Class D devices.

The MAX9775/MAX9776 utilize a fully differential architecture, a full-bridged output, and comprehensive click-and-pop suppression. A 3D stereo enhancement function allows the MAX9775 to widen the stereo sound field immersing the listener in a cleaner, richer sound experience than typically found in portable applications. The devices utilize a flexible, user-defined mixer architecture that includes an input mixer, volume control, and output mixer. All control is done through I^2C.

The mono receiver amplifier and stereo headphone amplifier use Maxim's patented† DirectDrive architecture that produces a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors, saving cost, space, and component height.

The MAX9775 is available in a 36-bump UCSP™ (3mm x 3mm) package. The MAX9776 is available in a 32-pin TQFN (5mm x 5mm) or a 36-bump UCSP (3mm x 3mm) package. Both devices are specified over the extended -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
VDDto GND	6V
PVDDto PGND	6V
CPVDDto CPGND	6V
CPVSSto CPGND	-6V to +0.3V
VSSto CPGND	-6V to +0.3V
C1N	(CPVSS- 0.3V) to (CPGND + 0.3V)
C1P	(CPGND - 0.3V) to (CPVDD+ 0.3V)
HPL, HPR to GND	(CPVSS- 0.3V) to (CPVDD+ 0.3V)
GND to PGND and CPGND	±0.3V
VDD to PVDDand CPVDD	±0.3V
SDA, SCL to GND	-0.3V to +6V
All other pins to GND	-0.3V to (VDD+ 0.3V)
Continuous Current In/Out of PVDD, PGND, CPVDD, CPGND,OUT__, HPR, and HPL.	±800mA
Continuous Input Current CPVSS	260mA
Continuous Input Current (all other pins)	±20mA
Duration of Short Circuit Between OUT_+ and OUT_-	Continuous
Duration of HP_, OUT_ Short Circuit to GND or PVDD	Continuous
Continuous Power Dissipation (TA= +70°C)	
36-Bump (3mm x 3mm) UCSP Multilayer Board	
Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°

II. Manufacturing Information

A. Description/Function: 2 x 1.5W, Stereo Class D Audio Subsystemwith DirectDrive Headphone Amplifier

B. Process: B6 (Standard 0.6 micron silicon gate CMOS)

C. Number of Device Transistors: 295

D. Fabrication Location: California, USA

E. Assembly Location: USA or Philippines

F. Date of Initial Production: February, 2007

III. Packaging Information

A. Package Type: **36-bump CSP**

B. Lead Frame: n/a

C. Lead Finish: n/a

D. Die Attach: n/a

E. Bondwire: n/a

F. Mold Material: n/a

G. Assembly Diagram: # 05-9000-2323

H. Flammability Rating: Class UL94-V0

IV. Die Information

A. Dimensions: 123 x 125 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 0.8 microns (as drawn)

F. Minimum Metal Spacing: 0.8 microns (as drawn)

G. Bondpad Dimensions: n/a

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.91 \times 10^{-9}$

$\lambda = 22.91$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the B6 Process results in a FIT Rate of 0.8 @ 25C and 14.2 @ 55C (0.8 eV, 60% UCL).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AU68-1 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX9775EBX

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality		77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		N/A	N/A
Mechanical Stress (Note 2 & 3)					
Temperature* Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: UCSP Temperature Cycle performed at -40°C/125°C, 1000 Cycles, ramp rate 11°C/minute, dwell=15 minutes, One cycle/hour

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

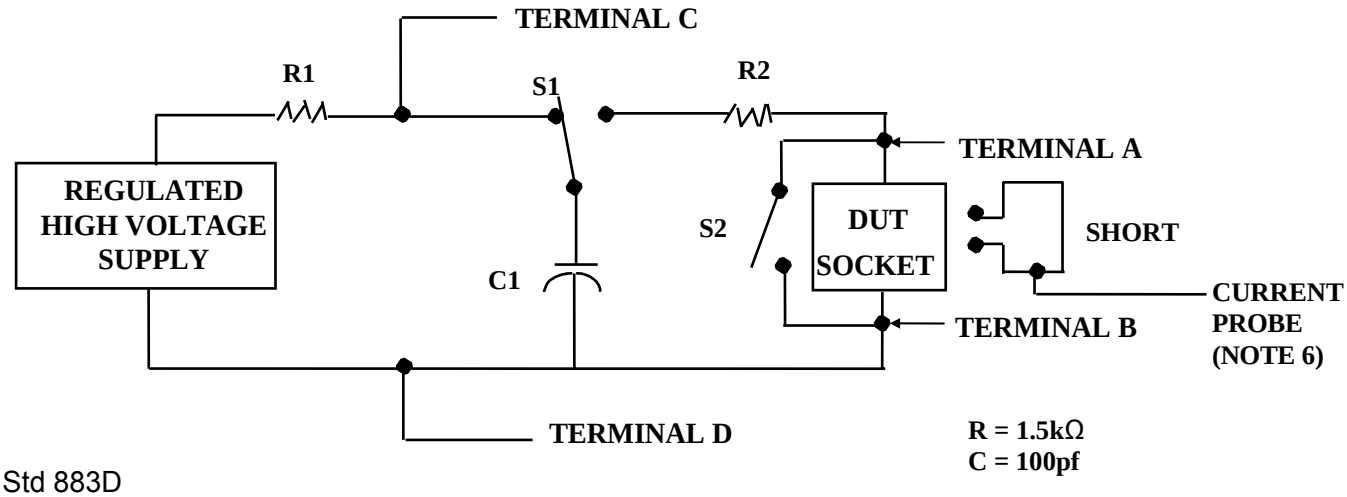
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

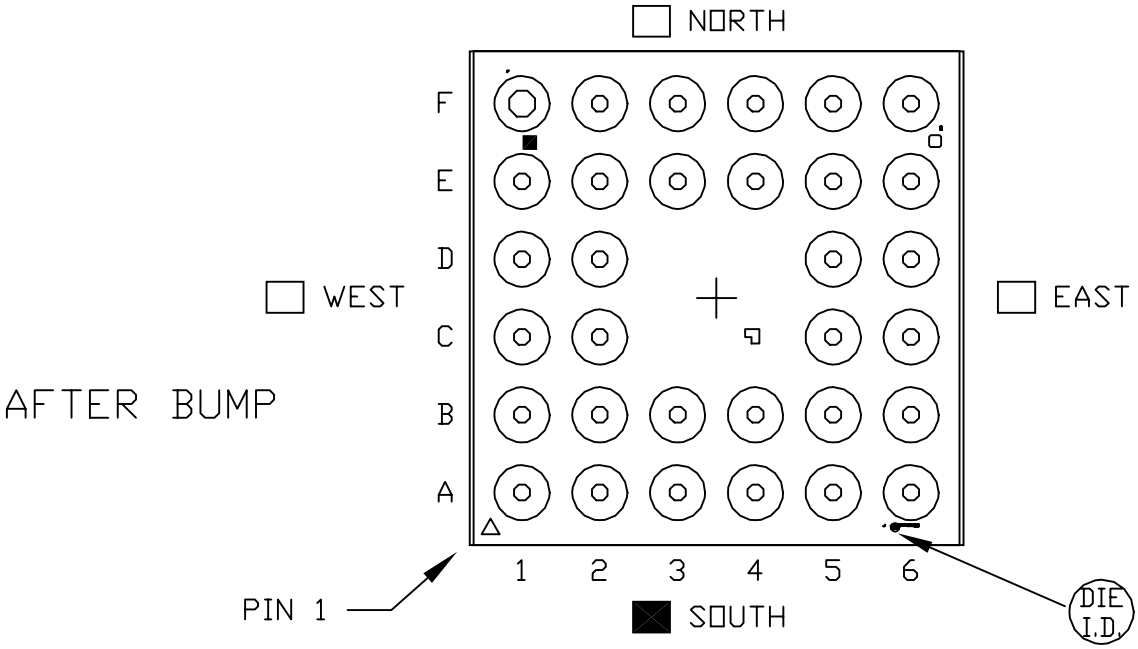
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

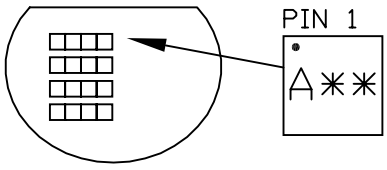
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.



PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)

PKG. CODE: B36-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: N/A	PKG.			BOND DIAGRAM #: 05-9000-2323	REV: B
	DESIGN				

AU68Z
MAX9775-MAX9776