RELIABILITY REPORT
FOR
MAX9602EUG
PLASTIC ENCAPSULATED DEVICES

June 27, 2003

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by  Reviewed by
Jim Pedicord  Bryan J. Preeshl
Quality Assurance  Quality Assurance
Reliability Lab Manager  Executive Director
Conclusion

The MAX9382 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

Table of Contents

I. Device Description     V. Quality Assurance Information
II. Manufacturing Information    VI. Reliability Evaluation
III. Packaging Information     IV. Die Information
      .....Attachments

I. Device Description

A. General

The MAX9602 ultra-high-speed comparator features extremely low propagation delay (500ps). This quad comparator minimizes propagation delay skew (10ps) and is designed for low propagation delay dispersion (30ps). These features make it ideal for applications where high-fidelity tracking of narrow pulses and low timing dispersion is critical.

The differential input stage accepts a wide range of signals in the common-mode range from $(V_{EE} + 3V)$ to $(V_{CC} - 2V)$. The outputs are complementary digital signals, compatible with ECL and PECL systems, and provide sufficient current to directly drive transmission lines terminated in $50\Omega$.

The MAX9602 quad-channel PECL output comparator is ideal for high-density packaging in limited board space.

The MAX9602 is offered in a 24-pin TSSOP package and is specified for operation from -40°C to +85°C.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VS = $V_{CC} - V_{EE}$</td>
<td>12.0V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>±6.5V</td>
</tr>
<tr>
<td>Latch Differential Voltage</td>
<td>±4V</td>
</tr>
<tr>
<td>Common-Mode Input Voltage (VCM)</td>
<td>$V_{EE}$ to $V_{CC}$</td>
</tr>
<tr>
<td>$V_{CCO_1}$ to $V_{EE}$</td>
<td>($V_{EE} - 0.3V$) to ($V_{CC} + 0.3V$)</td>
</tr>
<tr>
<td>$LE_1$, $LE_2$ to GND</td>
<td></td>
</tr>
<tr>
<td>Input Current to Any Input Pin</td>
<td>10mA</td>
</tr>
<tr>
<td>Continuous Output Current</td>
<td>50mA</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td>975mW</td>
</tr>
<tr>
<td>24-Pin TSSOP</td>
<td></td>
</tr>
<tr>
<td>Derate above +70°C</td>
<td>12.2mW/°C</td>
</tr>
<tr>
<td>24-Pin TSSOP</td>
<td></td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: Quad ECL and Quad PECL, 500ps, Ultra-High-Speed Comparators
B. Process: GST2 – High Speed Double Poly-Silicon Bipolar Process
C. Number of Device Transistors: 608
D. Fabrication Location: Oregon, USA
E. Assembly Location: Philippines or Malaysia
F. Date of Initial Production: March, 2002

III. Packaging Information

A. Package Type: 24-Pin TSSOP
B. Lead Frame: Copper
C. Lead Finish: Solder Plate
D. Die Attach: Silver-filled Epoxy
E. Bondwire: Gold (1.0 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: # 05-1501-0264
H. Flammability Rating: Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 59 x 87 mils
B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect: Poly / Au
D. Backside Metallization: None
E. Minimum Metal Width: 2 microns (as drawn)
F. Minimum Metal Spacing: 2 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO₂
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 45 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 10.78 \times 10^{-9}$$

$$\lambda = 10.78 \text{ F.I.T.} \ (60\% \ confidence \ level \ @ \ 25^\circ C)$$

This low failure rate represents data collected from Maxim’s reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. The attached Burn-In Schematic (Spec. # 06-5935) shows the static circuit used for this test. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-B2A).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The CM77 die type has been found to have all pins able to withstand a transient pulse of <200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.
### Table 1
Reliability Evaluation Test Results

**MAX9602EUG**

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong> (Note 1)</td>
<td><em>Ta = 150°C</em></td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>45</td>
<td>0</td>
</tr>
<tr>
<td><strong>Moisture Testing</strong> (Note 2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pressure Pot</td>
<td><em>Ta = 121°C</em></td>
<td>DC Parameters &amp; functionality</td>
<td>TSSOP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td><em>P = 15 psi.</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><em>RH = 100%</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><em>Time = 168hrs.</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>85/85</td>
<td><em>Ta = 85°C</em></td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td><em>RH = 85%</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><em>Time = 1000hrs.</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong> (Note 2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Cycle</td>
<td>-65°C/150°C</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1000 Cycles</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Method 1010</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Note 1: Life Test Data may represent plastic DIP qualification lots.*

*Note 2: Generic Package/Process data*
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th></th>
<th>Terminal A</th>
<th>Terminal B</th>
<th>(The common combination of all like-named pins connected to terminal B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
<td></td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
<td></td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.
DEVICES: MAX9602
PACKAGE: 24-TSSOP
MAX. EXPECTED CURRENT = +5V(170mA), -5V(50mA), +3V(130mA)

NOTES:

ONCE PER SOCKET

ONCE PER BOARD

DRAWN BY: HAK TAN