RELIABILITY REPORT

FOR

MAX931xxA

PLASTIC ENCAPSULATED DEVICES

July 24, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Conclusion

The MAX931 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX931 micropower, low-voltage comparator plus an on-board 2% accurate reference features the lowest power consumption available. This comparator includes an internal 1.182V ±2% voltage reference, programmable hysteresis, and TTL/CMOS outputs that sink and source current.

Ideal for 3V or 5V single-supply applications, the MAX931 operates from a single +2.5V to +11V supply (or a ±1.25V to ±5V dual supply), and each comparator's input voltage range extends from the negative supply rail to within 1.3V of the positive supply.

The MAX931 unique output stage continuously sources as much as 40mA. And by eliminating power-supply glitches that commonly occur when comparators change logic states, the MAX931 minimizes parasitic feedback, making it easier to use. The single MAX931 provides a unique and simple method for adding hysteresis without feedback and complicated equations, using the HYST pin and two resistors.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ to V-, V+ to GND, GND to V-</td>
<td>-0.3V, +12V</td>
</tr>
<tr>
<td>Inputs</td>
<td></td>
</tr>
<tr>
<td>Current, IN_+ , IN_-, HYST</td>
<td>20mA</td>
</tr>
<tr>
<td>Voltage, IN_+ , IN_-, HYST</td>
<td>(V+ + 0.3V) to (V- − 0.3V)</td>
</tr>
<tr>
<td>Outputs</td>
<td></td>
</tr>
<tr>
<td>Current, REF</td>
<td>20mA</td>
</tr>
<tr>
<td>Current, OUT_</td>
<td>50mA</td>
</tr>
<tr>
<td>Voltage, REF</td>
<td>(V+ + 0.3V) to (V- − 0.3V)</td>
</tr>
<tr>
<td>Voltage, OUT_</td>
<td>(V+ + 0.3V) to (V- − 0.3V)</td>
</tr>
<tr>
<td>OUT_ Short-Circuit Duration (V+ ≥ 5.5V)</td>
<td>Continuous</td>
</tr>
<tr>
<td>Operating Temperature Ranges:</td>
<td></td>
</tr>
<tr>
<td>MAX931C</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>MAX931E</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10sec)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = 70°C)</td>
<td></td>
</tr>
<tr>
<td>8-Pin SO</td>
<td>471mW</td>
</tr>
<tr>
<td>8-Pin PDIP</td>
<td>727mW</td>
</tr>
<tr>
<td>8-Pin uMAX</td>
<td>330mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td></td>
</tr>
<tr>
<td>8-Pin SO</td>
<td>5.88mW/°C</td>
</tr>
<tr>
<td>8-Pin PDIP</td>
<td>9.09mW/°C</td>
</tr>
<tr>
<td>8-Pin uMAX</td>
<td>4.1mW/°C</td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: Ultra Low-Power, Low-Cost Comparator with 2% Reference

B. Process: S3 [(SG3) - Standard 3 micron silicon gate CMOS]

C. Number of Device Transistors: 164

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia, Thailand or Philippines

F. Date of Initial Production: October, 1994

III. Packaging Information

A. Package Type: 8 Lead SO 8 Lead PDIP 8 Lead uMax

B. Lead Frame: Copper Copper Copper

C. Lead Finish: Solder Plate Solder Plate Solder Plate

D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy Silver-filled Epoxy

E. Bondwire: Gold (1.0 mil dia.) Gold (1.3 mil dia.) Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler Epoxy with silica filler Epoxy with silica filler

G. Assembly Diagram: # 05-1501-0097 # 05-1501-0096 # 05-1501-0098

H. Flammability Rating: Class UL94-V0 Class UL94-V0 Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1 Level 1 Level 1

IV. Die Information

A. Dimensions: 58 x 61 mils

B. Passivation: $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 3 microns (as drawn)

F. Minimum Metal Spacing: 3 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO$_2$

I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:
   - Jim Pedicord (Manager, Reliability Operations)
   - Bryan Preeshl (Executive Director of QA)
   - Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

   \[ \lambda = \frac{1}{\text{MTTF} = \frac{192 \times 4389 \times 320 \times 2}{1.83}} \]

   Thermal acceleration factor assuming a 0.8eV activation energy

   \[ \lambda = 3.39 \times 10^{-9} \quad \lambda = 3.39 \text{ F.I.T. (60% confidence level @ 25°C)} \]

   This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5126) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

   Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

   The CM21 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA.
<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong> (Note 1)</td>
<td>Ta = 135°C Biased</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>584</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Moisture Testing</strong> (Note 2)</td>
<td>Pressure Pot</td>
<td>Ta = 121°C P = 15 psi. RH= 100%</td>
<td>DC Parameters &amp; functionality</td>
<td>PDIP</td>
<td>77</td>
</tr>
<tr>
<td></td>
<td>Time = 96 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ta = 85°C RH = 85% Biased</td>
<td>DC Parameters &amp; functionality</td>
<td>SO</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Time = 1000 hrs.</td>
<td></td>
<td>uMAX</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong> (Note 2)</td>
<td>Temperature Cycle</td>
<td>-65°C/150°C 1000 Cycles Method 1010</td>
<td>DC Parameters</td>
<td></td>
<td>77</td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic/Package process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Each pin individually connected to terminal A with the other floating)</td>
<td>(The common combination of all like-named pins connected to terminal B)</td>
</tr>
<tr>
<td>1. All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2. All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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**REGULATED HIGH VOLTAGE SUPPLY**

**TERMINAL C**

**TERMINAL A**

**TERMINAL B**

**TERMINAL D**

**DUT**

**SOCKET**

**CURRENT PROBE** (NOTE 6)

**SHORT**

R1

S1

R2

S2

C1

R = 1.5kΩ

C = 100pf

Mil Std 883D
Method 3015.7
Notice 8