RELIABILITY REPORT

FOR

MAX9203ExA

PLASTIC ENCAPSULATED DEVICES

May 25th, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by  Reviewed by

Jim Pedicord  Bryan J. Preeshl
Quality Assurance  Quality Assurance
Reliability Lab Manager  Executive Director
Conclusion

The MAX9203 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX9203 high-speed, low-power, comparator features TTL logic outputs with active internal pullups. Fast propagation delay (7ns typ at 5mV overdrive) makes this device ideal for fast A/D converters and sampling circuits, line receivers, V/F converters, and many other data-discrimination, signal restoration applications.

The comparator can be powered from separate analog and digital power supplies or from a single combined supply voltage. The analog input common-mode range includes the negative rail, allowing ground sensing when powered from a single supply. The MAX9203 consumes only 9mW per comparator when powered from a +5V supply.

The MAX9203 features output latches with TTL compatible inputs. The comparator output states are held when the latch inputs are driven low.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Supply Voltage (VCC - VEE)</td>
<td>+12V</td>
</tr>
<tr>
<td>Digital Supply Voltage (VDD)</td>
<td>+7V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>(VEE - 0.3V) to (VCC + 0.3V)</td>
</tr>
<tr>
<td>Common Mode Input Voltage</td>
<td>(VEE - 0.3V) to (VCC + 0.3V)</td>
</tr>
<tr>
<td>Latch Input Voltage</td>
<td>-0.3V to (VDD + 0.3V)</td>
</tr>
<tr>
<td>Output Short-Circuit Duration To GND</td>
<td>Continuous</td>
</tr>
<tr>
<td>To VDD</td>
<td>1min</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-45°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td>727mW</td>
</tr>
<tr>
<td>8-Pin SOT</td>
<td>471mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td>9.1mW/°C</td>
</tr>
<tr>
<td>8-Pin SOT</td>
<td>5.9mW/°C</td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: Low Cost, 7ns, Low-Power Voltage Comparators

B. Process: CB20

C. Number of Device Transistors: 116

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines, Malaysia, or Thailand

F. Date of Initial Production: April, 2001

III. Packaging Information

A. Package Type: 8-Lead Small Outline  8-Lead SOT

B. Lead Frame: Copper  Copper

C. Lead Finish: Solder Plate  Solder Plate

D. Die Attach: Silver-filled Epoxy  Non-Conductive Epoxy

E. Bondwire: Gold (1.0 mil dia.)  Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler  Epoxy with silica filler

G. Assembly Diagram: # 05-1501-0227  # 05-1501-0228

H. Flammability Rating: Class UL94-V0  Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1  Level 1

IV. Die Information

A. Dimensions: 77 x 24 mils

B. Passivation: Si$_3$N$_4$/SiO$_2$ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Si

D. Backside Metallization: None

E. Minimum Metal Width: Metal1: 6; Metal2: 8 microns (as drawn)

F. Minimum Metal Spacing: Metal1: 2; Metal2: 3 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO$_2$

I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
   Bryan Preeshl (Executive Director)
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

   $\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$

   (Chi square value for MTTF upper limit)

   $\lambda = 13.57 \times 10^{-9}$

   $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

   This low failure rate represents data collected from Maxim’s reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-3124) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

   Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

   The CM81 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.
### Table 1
Reliability Evaluation Test Results

**MAX9203ExA**

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong> (Note 1)</td>
<td>Ta = 135°C</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>80</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Moisture Testing</strong> (Note 2)</td>
<td>Ta = 121°C</td>
<td>DC Parameters &amp; functionality</td>
<td>SO</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Pressure Pot</td>
<td>P = 15 psi.</td>
<td></td>
<td>SOT</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>RH = 100%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 168hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>85/85</td>
<td>Ta = 85°C</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>RH = 85%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 1000hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong> (Note 2)</td>
<td>-65°C/150°C</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Temperature Cycle</td>
<td>Method 1010</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
### Attachment #1

<table>
<thead>
<tr>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Each pin individually</td>
<td>(The common combination</td>
</tr>
<tr>
<td>connected to terminal A</td>
<td>of all like-named pins</td>
</tr>
<tr>
<td>with the other floating)</td>
<td>connected to terminal B)</td>
</tr>
<tr>
<td>1. All pins except $V_{PS1}$</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2. All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

#### 3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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**Mil Std 883D**
**Method 3015.7**
**Notice 8**
USE NON-CONDUCTIVE EPOXY

NOTE: CAVITY DOWN

BONDABLE AREA

PKG. CODE: K8-5
CAV/PAD SIZE: 88x28

SIGNATURES

DATE

CONFIDENTIAL & PROPRIETARY

BOND DIAGRAM #: 05-1501-0227
REV: A
DEVICES: MAX 903

MAX. EXPECTED CURRENT = 1.6 mA (-5V) 2 mA (+5V)

NOTES:

ONCE PER SOCKET

ONCE PER BOARD

8-PDIP

2mA

+5V

0.1uF

1.6mA

-5V

0.1uF