RELIABILITY REPORT

FOR

MAX9142ExA

PLASTIC ENCAPSULATED DEVICES

February 19, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Reviewed by
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Quality Assurance
Executive Director
Conclusion

The MAX9142 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

Table of Contents

I. ........Device Description V. ........Quality Assurance Information
II. ........Manufacturing Information VI. ........Reliability Evaluation
III. .......Packaging Information
IV. .......Die Information

I. Device Description

A. General

The MAX9142 is a dual/quad high-speed comparator optimized for systems powered from a 3V or 5V supply. The device combines high speed, low power, and Rail-to-Rail® inputs. Propagation delay is 40ns, while supply current is only 150µA per comparator.

The input common-mode range of the MAX9142 extends beyond both power-supply rails. The outputs pull to within 0.3V of either supply rail without external pullup circuitry, making these devices ideal for interface with both CMOS and TTL logic. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The MAX9142 is a higher-speed, lower-power, and lower-cost upgrade to industry-standard comparator MAX942.

The MAX9142 is available in a 8-pin SOT23 and SO packages.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Ranges</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage (VCC to GND)</td>
<td>+6V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>-0.3V to (VCC + 0.3V)</td>
</tr>
<tr>
<td>Common-Mode Input Voltage to GND</td>
<td>-0.3V to (VCC + 0.3V)</td>
</tr>
<tr>
<td>Input/Output Short-Circuit Duration to VCC or GND</td>
<td>Continuous</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td></td>
</tr>
<tr>
<td>8-Pin SO</td>
<td>470.6mW</td>
</tr>
<tr>
<td>8-Pin SOT23</td>
<td>727mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td></td>
</tr>
<tr>
<td>8-Pin SO</td>
<td>5.9mW/°C</td>
</tr>
<tr>
<td>8-Pin SOT23</td>
<td>9.1mW/°C</td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description: 40ns, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparator
B. Process: CB30
C. Number of Device Transistors: 314
D. Fabrication Location: Oregon, USA
E. Assembly Location: Malaysia, Philippines or Thailand
F. Date of Initial Production: May, 2001

III. Packaging Information

A. Package Type: 8-Pin SOT23 8-Pin SO
B. Lead Frame: Copper Copper
C. Lead Finish: Solder Plate Solder Plate
D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy
E. Bondwire: Gold (1.0 mil dia.) Gold (1.0 mil dia.)
F. Mold Material: Epoxy with silica filler Epoxy with silica filler
G. Assembly Diagram: Buildsheet # 05-1501-0237 Buildsheet # 05-1501-0238
H. Flammability Rating: Class UL94-V0 Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1 Level 1

IV. Die Information

A. Dimensions: 76 x 24 mils
B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect: Gold
D. Backside Metallization: None
E. Minimum Metal Width: Metal 1: 1.4 microns Metal 2: 1.4 microns Metal 3: 3 microns (as drawn)
F. Minimum Metal Spacing: Metal 1: 1.6 microns Metal 2: 1.6 microns Metal 3: 3 microns (as drawn)
G. Bondpad Dimensions: 2.7 mil. Sq.
H. Isolation Dielectric: SiO₂
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:  Jim Pedicord (Reliability Lab Manager)
   Bryan Preeshl (Executive Director of QA)
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level:  0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate:  < 50 ppm

D. Sampling Plan:  Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

   \[
   \lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad \text{(Chi square value for MTTF upper limit)}
   \]

   Temperature Acceleration factor assuming an activation energy of 0.8eV

   \[
   \lambda = 13.57 \times 10^{-9} \quad \lambda = 13.57 \text{ F.I.T.} \quad (60\% \text{ confidence level } @ \ 25^\circ\text{C})
   \]

   This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5684) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

   Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

   The CM69 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.
# Table 1
## Reliability Evaluation Test Results

**MAX9142ExA**

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong> (Note 1)</td>
<td>Ta = 135°C</td>
<td>DC Parameters &amp; functionality</td>
<td>SOT23</td>
<td>80</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td>SO</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Moisture Testing</strong> (Note 2)</td>
<td>Ta = 121°C</td>
<td>DC Parameters &amp; functionality</td>
<td>SOT23</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Pressure Pot</td>
<td>P = 15 psi.</td>
<td></td>
<td>SO</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RH = 100%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 168hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>85/85</td>
<td>Ta = 85°C</td>
<td>DC Parameters &amp; functionality</td>
<td>SOT23</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>RH = 85%</td>
<td></td>
<td>SO</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 1000hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong> (Note 2)</td>
<td>Ta = -65°C/150°C</td>
<td>DC Parameters</td>
<td>SOT23</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Temperature Cycle</td>
<td>1000 Cycles</td>
<td></td>
<td>SO</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Method 1010</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Each pin individually connected to terminal A with the other floating)</td>
<td>(The common combination of all like-named pins connected to terminal B)</td>
</tr>
<tr>
<td>1.</td>
<td>All pins except V&lt;sub&gt;PS1&lt;/sub&gt; 3/</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V<sub>PS1</sub> is V<sub>DD</sub>, V<sub>CC</sub>, V<sub>SS</sub>, V<sub>BB</sub>, GND, +V<sub>S</sub>, -V<sub>S</sub>, V<sub>REF</sub>, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V<sub>SS1</sub>, or V<sub>SS2</sub> or V<sub>SS3</sub> or V<sub>CC1</sub>, or V<sub>CC2</sub>) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

---

**Attachment #1**

**TABLE II. Pin combination to be tested.**

<table>
<thead>
<tr>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Each pin individually connected to terminal A with the other floating)</td>
<td>(The common combination of all like-named pins connected to terminal B)</td>
</tr>
<tr>
<td>1. All pins except V&lt;sub&gt;PS1&lt;/sub&gt; 3/</td>
<td>All V&lt;sub&gt;PS1&lt;/sub&gt; pins</td>
</tr>
<tr>
<td>2. All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
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3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V<sub>PS1</sub> is V<sub>DD</sub>, V<sub>CC</sub>, V<sub>SS</sub>, V<sub>BB</sub>, GND, +V<sub>S</sub>, -V<sub>S</sub>, V<sub>REF</sub>, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V<sub>SS1</sub>, or V<sub>SS2</sub> or V<sub>SS3</sub> or V<sub>CC1</sub>, or V<sub>CC2</sub>) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

---

**Regulated High Voltage Supply**

**Terminal C**

**Terminal A**

**Terminal B**

**Terminal D**

R = 1.5kΩ
C = 100pf

**Mil Std 883D**
**Method 3015.7**
**Notice 8**
<table>
<thead>
<tr>
<th>PKG. CODE:</th>
<th>SIGNATURES</th>
<th>DATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>K8-5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CAV./PAD SIZE:</td>
<td>PKG.</td>
<td>DESIGN</td>
</tr>
<tr>
<td>88x28</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
ONCE PER SOCKET

DEVICES: MAX 9142/9107/LMX393/393H

MAX. EXPECTED CURRENT = 1.6 mA

NOTES:

+ 5 VOLTS

10 OHMS

0.1 uF

8 PIN SOT