RELIABILITY REPORT
FOR
MAX903xxA
PLASTIC ENCAPSULATED DEVICES

May 15th, 2003

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

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Conclusion

The MAX903 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

Table of Contents

I. ........Device Description                                            V. ........Quality Assurance Information
II. ........Manufacturing Information                                   VI. ........Reliability Evaluation
III. .......Packaging Information                                      ......Attachments
IV. .......Die Information

I.  Device Description

A.  General

The MAX903 single, high-speed, low-power, dual voltage comparator features differential analog input and TTL logic output with active internal pull-up. Fast propagation delay (8ns typ at 5mV overdrive) makes the MAX902 ideal for fast A/D converters and sampling circuits, line receivers, V/F converters, and many other data-discrimination applications.

The comparator can be powered from separate analog and digital power supplies or from a single combined supply voltage. The analog input common-mode range includes the negative rail, allowing ground sensing when powered from a single supply. The MAX903 consumes 18mW per comparator when powered from +5V.

The MAX903 is equipped with independent TTL compatible latch input. The comparator output state is held when the latch input is driven low.

B.  Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Supply Voltage (V_{CC} to V_{EE})</td>
<td>+12V</td>
</tr>
<tr>
<td>Digital Supply Voltage (V_{DD} to GND)</td>
<td>+7V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>(V_{EE} - 0.2V) to (V_{CC} + 0.2V)</td>
</tr>
<tr>
<td>Common-Mode Input Voltage</td>
<td>(V_{EE} - 0.2V) to (V_{CC} + 0.2V)</td>
</tr>
<tr>
<td>Latch Input Voltage</td>
<td>-0.2V to (V_{DD} + 0.2V)</td>
</tr>
<tr>
<td>Output Short-Circuit Duration</td>
<td></td>
</tr>
<tr>
<td>to GND</td>
<td>Indefinite</td>
</tr>
<tr>
<td>to V_{DD}</td>
<td>1 min</td>
</tr>
<tr>
<td>Storage Temp.</td>
<td>-65°C to +160°C</td>
</tr>
<tr>
<td>Lead Temp. (10 sec.)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>500mW</td>
</tr>
<tr>
<td>Derates above +100°C</td>
<td>10mW/°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td></td>
</tr>
<tr>
<td>8-Pin SO</td>
<td>471mW</td>
</tr>
<tr>
<td>8-Pin DIP</td>
<td>727mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td></td>
</tr>
<tr>
<td>8-Pin SO</td>
<td>5.9mW/°C</td>
</tr>
<tr>
<td>8-Pin DIP</td>
<td>9.1mW/°C</td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: Single High-Speed, Low-Power Voltage Comparator
B. Process: CB20
C. Number of Device Transistors: 65
D. Fabrication Location: Oregon, USA
E. Assembly Location: Philippines, Malaysia, or Thailand
F. Date of Initial Production: June, 1991

III. Packaging Information

A. Package Type:
   - 8-Lead Small Outline
   - 8-Lead DIP
B. Lead Frame: Copper
C. Lead Finish: Solder Plate
D. Die Attach: Silver-filled Epoxy
E. Bondwire: Gold (1.0 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: # 05-1501-0228
H. Flammability Rating: Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 77 x 24 mils
B. Passivation: Si$_3$N$_4$/SiO$_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect: Aluminum/Copper/Si
D. Backside Metallization: None
E. Minimum Metal Width: Metal1: 6; Metal2: 8 microns (as drawn)
F. Minimum Metal Spacing: Metal1: 2; Metal2: 3 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO$_2$
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:  
   Jim Pedicord (Manager, Rel Operations)  
   Bryan Preeshl (Executive Director)  
   Kenneth Huening (Vice President)  

B. Outgoing Inspection Level:   0.1% for all electrical parameters guaranteed by the Datasheet.  
                                0.1% For all Visual Defects.  

C. Observed Outgoing Defect Rate:  < 50 ppm  

D. Sampling Plan:  Mil-Std-105D  

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure  
   Rate ($\lambda$) is calculated as follows:  

   $\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$  
   \[\text{(Chi square value for MTTF upper limit)}\]  
   
   $\lambda = \frac{1}{\text{MTTF}}$  
   \[\text{Temperature Acceleration factor assuming an activation energy of 0.8eV}\]  

   $\lambda = 13.57 \times 10^{-9}$  

   $\lambda = 13.57 \text{ F.I.T. (60% confidence level @ 25°C)}$  

   This low failure rate represents data collected from Maxim’s reliability monitor program. In addition to  
   routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects  
   it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be  
   shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece  
   sample. Attached Burn-In Schematic (Spec. # 06-3124) shows the static Burn-In circuit. Maxim performs failure  
   analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test  
   monitors. This data is published in the Product Reliability Report (RR-1M).  

B. Moisture Resistance Tests

   Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample  
   must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard  
   85°C/85%RH testing is done per generic device/package family once a quarter.  

C. E.S.D. and Latch-Up Testing

   The CM81 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500$V, per Mil-  
   Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device  
   withstands a current of $\pm 250$mA.
<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test</td>
<td>Ta = 135°C</td>
<td>DC Parameters</td>
<td>SO</td>
<td>80</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td>&amp; functionality</td>
<td>PDIP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Moisture Testing</td>
<td>Ta = 121°C</td>
<td>DC Parameters</td>
<td>SO</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>P = 15 psi.</td>
<td>&amp; functionality</td>
<td>PDIP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>RH = 100%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 168 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ta = 85°C</td>
<td>DC Parameters</td>
<td>SO</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>RH = 85%</td>
<td>&amp; functionality</td>
<td>PDIP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 1000 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mechanical Stress</td>
<td>-65°C/150°C</td>
<td>DC Parameters</td>
<td>SO</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1000 Cycles</td>
<td>&amp; functionality</td>
<td>PDIP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Method 1010</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th></th>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_{S}$, $-V_{S}$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.
DEVICES: MAX 903

MAX. EXPECTED CURRENT = 1.6 mA (-5V) 2 mA (+5V)

NOTES:

1. ONCE PER SOCKET
2. ONCE PER BOARD

DRAWN BY: HAK TAN