RELIABILITY REPORT
FOR
MAX865EUA
PLASTIC ENCAPSULATED DEVICES

March 6, 2003

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by  Reviewed by
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Quality Assurance  Quality Assurance
Reliability Lab Manager  Executive Director
Conclusion

The MAX865 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX865 is a CMOS charge-pump DC-DC converter in an ultra-small μMAX package. It produces positive and negative outputs from a single positive input, and requires only four capacitors. The charge pump first doubles the input voltage, then inverts the doubled voltage. The input voltage ranges from +1.5V to +6.0V.

The internal oscillator is guaranteed to be between 20kHz and 38kHz, keeping noise above the audio range while consuming minimal supply current. A 75Ω output impedance permits useful output currents up to 20mA.

The 1.11mm-high, 8-pin μMAX package occupies half the board area of a standard 8-pin SOIC.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ to GND</td>
<td>+12V, -3V</td>
</tr>
<tr>
<td>IN to GND</td>
<td>+6.2V, -0.3V</td>
</tr>
<tr>
<td>V- to GND</td>
<td>-12V, +0.3V</td>
</tr>
<tr>
<td>V- Output Current</td>
<td>100mA</td>
</tr>
<tr>
<td>V- Short Circuit to GND</td>
<td>Indefinite</td>
</tr>
<tr>
<td>Storage Temp.</td>
<td>-65°C to +160°C</td>
</tr>
<tr>
<td>Lead Temp. (10 sec.)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>330mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td>4.1mW/°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td>330mW</td>
</tr>
<tr>
<td>8-Pin μMAX</td>
<td></td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td>4.1mW/°C</td>
</tr>
<tr>
<td>8-Pin μMAX</td>
<td></td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: Compact, Dual-Output Charge Pump
B. Process: M5 (5 micron metal gate CMOS)
C. Number of Device Transistors: 80
D. Fabrication Location: Oregon, USA
E. Assembly Location: Malaysia, Thailand or Philippines
F. Date of Initial Production: February, 1996

III. Packaging Information

A. Package Type: 8-Lead uMAX
B. Lead Frame: Copper
C. Lead Finish: Solder Plate
D. Die Attach: Silver-filled Epoxy
E. Bondwire: Gold (1.3 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: # 05-1701-0275
H. Flammability Rating: Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 58x84 mils
B. Passivation: SiN/SiO (nitride/oxide)
C. Interconnect: Aluminum/Si (Si = 1%)
D. Backside Metallization: None
E. Minimum Metal Width: 5 microns (as drawn)
F. Minimum Metal Spacing: 5 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO₂
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
   Bryan Preeshl (Executive Director of QA)
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

   $\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$  (Chi square value for MTTF upper limit)

   Temperature Acceleration factor assuming an activation energy of 0.8eV

   $\lambda = 6.79 \times 10^{-9}$, $\lambda = 6.79$ F.I.T.  (60% confidence level @ 25°C)

   This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5140) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

   Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

   The PW83-2 die type has been found to have all pins able to withstand a transient pulse of ±3000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±150mA.
<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong> (Note 1)</td>
<td>Ta = 135°C Biased \nTime = 192 hrs.</td>
<td>DC Parameters \n&amp; functionality</td>
<td></td>
<td>160</td>
<td>0</td>
</tr>
<tr>
<td><strong>Moisture Testing</strong> (Note 2)</td>
<td>Pressure Pot \nTa = 121°C \nP = 15 psi. \nRH = 100% \nTime = 168hrs.</td>
<td>DC Parameters \n&amp; functionality</td>
<td>uMAX</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>85/85</td>
<td>Ta = 85°C \nRH = 85% \nBiased \nTime = 1000hrs.</td>
<td>DC Parameters \n&amp; functionality</td>
<td>77</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong> (Note 2)</td>
<td>Temperature Cycle \n-65°C/150°C \n1000 Cycles \nMethod 1010</td>
<td>DC Parameters</td>
<td>77</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th></th>
<th>Terminal A (Each pin individually connected to terminal A with the other floating)</th>
<th>Terminal B (The common combination of all like-named pins connected to terminal B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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Mil Std 883D
Method 3015.7
Notice 8