RELIABILITY REPORT

FOR

MAX8212xxx

PLASTIC ENCAPSULATED DEVICES

March 23, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by  Reviewed by

Jim Pedicord  Bryan J. Preeshl
Quality Assurance  Quality Assurance
Reliability Lab Manager  Executive Director
Conclusion

The MAX8212 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

Maxim’s MAX8212 is a CMOS micropower voltage detector that warns microprocessors (µPs) of power failures. The MAX8212 contains a comparator, a 1.15V bandgap reference, and open drain N-channel output driver. Two external resistors are used in conjunction with the internal reference to set the trip voltage to the desired level. A Hysteresis output is also included, allowing the user to apply positive feedback for noise-free output switching.

In the MAX8212, a voltage greater than 1.5V at the threshold pin turns the output stage on (no current limit).

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>-0.5V to +18V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>-0.5V to +18V</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>+0.5V to -18V with respect to (V+ + 0.5V)</td>
</tr>
<tr>
<td>Threshold Input Voltage</td>
<td>-0.5V to (V+ + 0.5V)</td>
</tr>
<tr>
<td>Current into Any Terminal</td>
<td>±50mA</td>
</tr>
<tr>
<td>Operating Temperature Ranges</td>
<td></td>
</tr>
<tr>
<td>MAX8212C_ _</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>MAX8212E_ _</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10sec)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td></td>
</tr>
<tr>
<td>8-Pin PDIP</td>
<td>727mW</td>
</tr>
<tr>
<td>8-Pin SO</td>
<td>471mW</td>
</tr>
<tr>
<td>8-Pin uMAX</td>
<td>330mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td></td>
</tr>
<tr>
<td>8-Pin PDIP</td>
<td>9.09mW/°C</td>
</tr>
<tr>
<td>8-Pin SO</td>
<td>5.88mW/°C</td>
</tr>
<tr>
<td>8-Pin uMAX</td>
<td>4.1mW/°C</td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: Programmable Voltage Detector

B. Process: M6 (6 micron metal gate CMOS)

C. Number of Device Transistors: 30

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines, Malaysia, or Thailand

F. Date of Initial Production: November, 1993

III. Packaging Information

A. Package Type: 8-Lead Plastic Dip, 8-Lead SO, 8-Lead uMAX

B. Lead Frame: Copper, Copper, Copper

C. Lead Finish: Solder Plate, Solder Plate, Solder Plate

D. Die Attach: Silver-filled Epoxy, Silver-filled Epoxy, Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.), Gold (1.0 mil dia.), Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler, Epoxy with silica filler, Epoxy with silica filler

G. Assembly Diagram: # 05-0701-0296, # 05-0701-0297, # 05-0701-0764

H. Flammability Rating: Class UL94-V0, Class UL94-V0, Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1, Level 1, Level 1

IV. Die Information

A. Dimensions: 57 x 69 mils

B. Passivation: Si$_3$N$_4$/SiO$_2$ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 6 microns (as drawn)

F. Minimum Metal Spacing: 6 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO$_2$

I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:
   Jim Pedicord (Reliability Lab Manager)
   Bryan Preeshl (Executive Director)
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level:
   0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 400 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 2.71 \times 10^{-9}$$

$$\lambda = 2.71 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim’s reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-1797) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PS50-1 die type has been found to have all pins able to withstand a transient pulse of ±800V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA.
<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test (Note 1)</td>
<td>Ta = 135°C Biased Time = 192 hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>400</td>
<td>0</td>
</tr>
<tr>
<td>Moisture Testing (Note 2)</td>
<td>Pressure Pot Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td>PDIP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>85/85 Ta = 85°C RH = 85% Biased Time = 1000hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td>SO</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>uMAX</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Mechanical Stress (Note 2)</td>
<td>Temperature Cycle -65°C/150°C 1000 Cycles Method 1010</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th></th>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(Each pin individually</td>
<td>(The common combination of all like-named pins</td>
</tr>
<tr>
<td></td>
<td>connected to terminal A</td>
<td>connected to terminal B)</td>
</tr>
<tr>
<td></td>
<td>with the other floating)</td>
<td></td>
</tr>
<tr>
<td>1.</td>
<td>All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground
   (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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Mil Std 883D
Method 3015.7
Notice 8
NOTES:
1. TEMPERATURE: 125°C OR EQUIVALENT
2. TIME: 150 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 125°C CONTINUOUS
4. APPROVED FOR (0) COMMERCIAL
   (0) HR/800

SPEC. NO. 06-1797 REV. A

MAXIM BURN-IN SCHEMATIC

DATE: 6/25/92

DRAWN BY: N.K. NGUYEN

DEVICE TYPE:
MAX3211/2