RELIABILITY REPORT
FOR
MAX6464xxxx
PLASTIC ENCAPSULATED DEVICES

February 2, 2004

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by  Reviewed by
Jim Pedicord  Bryan J. Preeshl
Quality Assurance  Quality Assurance
Reliability Lab Manager  Executive Director
Conclusion

The MAX6464 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX6464 µP reset supervisory circuit monitors battery, power-supply, and system voltages. The circuit includes a precision bandgap reference, a comparator, internally trimmed resistor networks that set specified trip thresholds, and an internal 5% threshold hysteresis circuit (see the Functional Diagram). Output is asserted when \( V_{CC} \) falls below the internal \( V_{TH}^- \) and remains asserted until \( V_{CC} \) rises above \( V_{TH}^+ \) (\( V_{TH}^+ = V_{TH}^- \times 1.05 \)). This device provides excellent circuit reliability and low cost by eliminating external components and adjustments when monitoring nominal system voltages from +1.6V to +5.5V.

The MAX6464 is a µP supervisory circuit with a minimum reset timeout period of 150ms. The device is available with thresholds from +1.6V to +5.5V in 100mV increments.

The device is available with a push-pull with active-low output three output stage. The device is available in SC70 and SOT23 packages specified over the -40°C to +125°C temperature range.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>-0.3V to +7V</td>
</tr>
<tr>
<td>Push-Pull OUT/OUT</td>
<td>-0.3V to (VCC + 0.3V)</td>
</tr>
<tr>
<td>Input/Output Current (all pins)</td>
<td>20mA</td>
</tr>
<tr>
<td>Output Short Circuit (VCC or GND)</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +125°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td>228.6mW</td>
</tr>
<tr>
<td>3-Pin SC70</td>
<td>320mW</td>
</tr>
<tr>
<td>3-Pin SOT23</td>
<td>571mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td>2.9mW/°C</td>
</tr>
<tr>
<td>3-Pin SC70</td>
<td>4.0mW/°C</td>
</tr>
<tr>
<td>3-Pin SOT23</td>
<td>7.1mW/°C</td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: Ultra-Low-Power µP Supervisory Circuits
B. Process: S8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors: 581
D. Fabrication Location: California, USA
E. Assembly Location: Malaysia or Thailand
F. Date of Initial Production: July, 2002

III. Packaging Information

A. Package Type:
   - 3-Pin SOT23
   - 3-Pin SC70
   - 5-Pin SOT23
B. Lead Frame:
   - Alloy 42
   - Copper or Alloy 42
   - Copper
C. Lead Finish:
   - Solder Plate
   - Solder Plate
   - Solder Plate
D. Die Attach:
   - Non-Conductive
   - Non-Conductive
   - Silver-filled Epoxy
E. Bondwire:
   - Gold (1 mil dia.)
   - Gold (1 mil dia.)
   - Gold (1 mil dia.)
F. Mold Material:
   - Epoxy with silica filler
   - Epoxy with silica filler
   - Epoxy with silica filler
G. Assembly Diagram:
   - # 05-1601-0195
   - # 05-1601-0194
   - # 05-1601-0192
H. Flammability Rating:
   - Class UL94-V0
   - Class UL94-V0
   - Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:
   - Level 1
   - Level 1
   - Level 1

IV. Die Information

A. Dimensions: 30 x 31 mils
B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect: Aluminum/Si (Si = 1%)
D. Backside Metallization: None
E. Minimum Metal Width: 0.8 microns (as drawn)
F. Minimum Metal Spacing: 0.8 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO₂
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:
   Jim Pedicord (Manager, Reliability Operations)
   Bryan Preeshl (Executive Director)
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level:
   0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

   \[
   \lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad \text{(Chi square value for MTTF upper limit)}
   \]

   \[
   \lambda = \frac{1}{192 \times 4389 \times 80 \times 2} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad \text{Temperature Acceleration factor assuming an activation energy of 0.8eV}
   \]

   \[
   \lambda = 13.57 \times 10^{-9}
   \]

   \[
   \lambda = 13.57 \text{ F.I.T. (60% confidence level @ 25°C)}
   \]

   This low failure rate represents data collected from Maxim’s reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5681) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

   Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

   The MS81-3 die type has been found to have all pins able to withstand a transient pulse of ±2500V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.
## Table 1
Reliability Evaluation Test Results

### MAX6464xxxx

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong> (Note 1)</td>
<td>$T_a = 135^\circ C$ Biased Time = 192 hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>80</td>
<td>0</td>
</tr>
<tr>
<td><strong>Moisture Testing</strong> (Note 2)</td>
<td>$T_a = 121^\circ C$ P = 15 psi. RH= 100% Time = 168hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td>SOT23</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>$T_a = 85^\circ C$ RH = 85% Biased Time = 1000hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td>SC70</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong> (Note 2)</td>
<td>$-65^\circ C/150^\circ C$ 1000 Cycles Method 1010</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th>Terminal A (Each pin individually connected to terminal A with the other floating)</th>
<th>Terminal B (The common combination of all like-named pins connected to terminal B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2. All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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Mil Std 883D
Method 3015.7
Notice 8
USE NON-CONDUCTIVE EPOXY

BONDING AREA

PKG. CODE: U3-1

CAV./PAD SIZE: 45x32

SIGNATURES

PKG.

DESIGN

DATE

BOND DIAGRAM #: 05-1601-0195

REV: A

CONFIDENTIAL & PROPRIETARY
USE NON-CONDUCTIVE EPOXY

SCALE: 40x

CAVITY DOWN

BONDABLE AREA

PKG. CODE: X3-2
CAV./PAD SIZE: 34x35

SIGNATURES

DATE

BOND DIAGRAM #: 05-1601-0194

REV: A
0 - BONDING AREA

NOTE: CAVITY DOWN

PKG. CODE: U5-1

PKG. SIZE: 64x45

SIGNATURES

DATE

MAXIM
CONFIDENTIAL & PROPRIETARY

BOND DIAGRAM #: 05-1601-0192

REV: A
DEVICES: MAX 9021/ MAX 9031/6461/6841
MAX. EXPECTED CURRENT = 5μA (MAX 9021) 50μA (MAX9031)
2.5μA (MAX6461) 40μA (MAX6841).

NOTES:
- ONCE PER SOCKET
- ONCE PER BOARD

- +5V
- 10 OHMS

+IN
VDD
GND
- IN
OUT
SOT23-5