RELIABILITY REPORT

FOR

MAX6394US480D3+T

PLASTIC ENCAPSULATED DEVICES

July 11, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX6394US480D3+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX6394 low-power CMOS microprocessor (µP) supervisory circuit is designed to monitor power supplies in µP and digital systems. It offers excellent circuit reliability by providing 1% accurate thresholds over temperature and by eliminating external components and adjustments. The MAX6394 also provides a debounced manual reset input. This device performs a single function: it asserts a reset signal whenever the VCC supply voltage falls below a preset threshold or whenever manual reset is asserted. Active-low RESET remains asserted for an internally programmed interval (reset timeout period) after VCC has risen above the reset threshold or manual reset is deasserted. The MAX6394's open-drain active-low RESET output can be pulled up to a voltage higher than VCC. The MAX6394 comes with factory-trimmed reset threshold voltages from 2.4V to 4.8V. Preset timeout periods of 0.7ms, 14ms, 105ms, and 826ms are also available. The device comes in a SOT143 package.

II. Manufacturing Information

A. Description/Function:	High-Accuracy µP Reset Circuit
B. Process:	B12
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Thailand
F. Date of Initial Production:	January 24, 2008

III. Packaging Information

A. Package Type:	4-pin SOT
B. Lead Frame:	Alloy42
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1601-0131
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Jb:	250*°C/W
K. Single Layer Theta Jc:	130°C/W
L. Multi Layer Theta Ja:	290°C/W
M. Multi Layer Theta Jc:	100°C/W

IV. Die Information

A. Dimensions:	40 X 31 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 139 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 1.5 \times 10^{-9}$

λ = 1.5 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the B12 Process results in a FIT Rate of 0.06 @ 25C and 1.06 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot JNMBLA023A, D/C 1022)

The MS11-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX6394US480D3+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	77	0	NNMBKA005H, D/C 0643
	Biased	& functionality	62	0	NNMBFA063B, D/C N/A
	Time = 1000 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.