RELIABILITY REPORT
FOR
MAX619xxA
PLASTIC ENCAPSULATED DEVICES

March 31, 2004

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
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Executive Director
Conclusion

The MAX619 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX619 step-up charge pump DC-DC converter delivers a regulated 5V ±4% output at 50mA over temperature. The input voltage range is 2V to 3.6V (two battery cells).

The complete MAX619 circuit fits into less than 0.1in\(^2\) of board space because it requires only four external capacitors: two 0.22\(\mu\)F flying capacitors, and 10\(\mu\)F capacitors at the input and output.

Low operating supply current (150\(\mu\)A max) and low shutdown supply current (1\(\mu\)A max) make this device ideal for small, portable, and battery-powered applications. When shut down, the load is disconnected from the input.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IN}) to GND</td>
<td>-0.3V to +5.5V</td>
</tr>
<tr>
<td>(V_{OUT}) to GND</td>
<td>-0.3V to +5.5V</td>
</tr>
<tr>
<td>SHDN to GND</td>
<td>-0.3V to ((V_{IN} + 0.3V))</td>
</tr>
<tr>
<td>(I_{OUT}) Continuous (Note 1)</td>
<td>120mA</td>
</tr>
<tr>
<td>Storage Temp.</td>
<td>-65°C to +165°C</td>
</tr>
<tr>
<td>Lead Temp. (10 sec.)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td>762mW</td>
</tr>
<tr>
<td>8-Pin PDIP</td>
<td>762mW</td>
</tr>
<tr>
<td>8-Pin NSO</td>
<td>9.4mW/°C</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td>9.4mW/°C</td>
</tr>
<tr>
<td>8-Pin PDIP</td>
<td></td>
</tr>
<tr>
<td>8-Pin NSO</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: The MAX619 is not short-circuit protected.
II. Manufacturing Information

A. Description/Function: Regulated 5V Charge-Pump DC-DC Converter

B. Process: SG1.2 (Standard 1.2 micron silicon gate CMOS)

C. Number of Device Transistors: 599

D. Fabrication Location: California or Oregon, USA

E. Assembly Location: Philippines, Malaysia, or Thailand

F. Date of Initial Production: February, 1994

III. Packaging Information

A. Package Type: 8-Lead NSO 8-Lead PDIP

B. Lead Frame: Copper Copper

C. Lead Finish: Solder Plate Solder Plate

D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.) Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler Epoxy with silica filler

G. Assembly Diagram: # 05-2301-0002 # 05-2301-0001

H. Flammability Rating: Class UL94-V0 Class UL94-V0

I. Classification of Moisture Sensitivity
   Per JEDEC standard J-STD-022A: Level 1 Level 1

IV. Die Information

A. Dimensions: 70 x 84 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Si

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For All Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$  (Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 13.57 \times 10^{-9} \quad \lambda = 13.57 \text{ F.I.T.} \quad (60\% \text{ confidence level @ 25°C})$$

This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5039) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PY02 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500V$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250mA$. 
<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test</td>
<td>Ta = 135°C</td>
<td>DC Parameters</td>
<td>PDIP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td>192 hrs.</td>
<td></td>
</tr>
<tr>
<td>Moisture Testing</td>
<td>Ta = 121°C</td>
<td>DC Parameters</td>
<td>NSO</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>P = 15 psi.</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RH = 100%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 168 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>85/85</td>
<td>Ta = 85°C</td>
<td>DC Parameters</td>
<td>PDIP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>RH = 85%</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 1000 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mechanical Stress</td>
<td>-65°C/150°C</td>
<td>DC Parameters</td>
<td>PDIP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Cycle</td>
<td>1000 Cycles</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Method 1010</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data
TABLE II. Pin combination to be tested.  

<table>
<thead>
<tr>
<th></th>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(Each pin individually connected to terminal A</td>
<td>(The common combination of all like-named pins</td>
</tr>
<tr>
<td></td>
<td>with the other floating)</td>
<td>connected to terminal B)</td>
</tr>
<tr>
<td>1.</td>
<td>All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.