

RELIABILITY REPORT
FOR
MAX6071xxAUTxx+T
PLASTIC ENCAPSULATED DEVICES

December 19, 2012

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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Conclusion

The MAX6071xxAUTxx+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX6070/MAX6071 offer a very low noise and low-drift voltage reference in a small 6-pin SOT23 package. These devices provide a 1/f noise voltage of only $4.8\mu\text{V}_{\text{p-p}}$ at an output voltage of 2.5V, with a temperature drift of 6ppm/°C (max). The devices operate with an input voltage from 2.8V to 5.5V. The MAX6070/MAX6071 consume 150 μA of supply current and can sink and source up to 10mA of load current. The MAX6070/MAX6071 provide an initial accuracy of 0.04%. The low-drift and low-noise specifications enable enhanced system accuracy, making these devices ideal for high precision industrial applications. The MAX6070 offers a noise filter option for wideband applications. The MAX6070/MAX6071 provide output voltages of 1.25V, 2.5V, and 4.096V. The devices are available in a 6-pin SOT23 package and specified over the extended industrial temperature range of -40°C to +125°C.

II. Manufacturing Information

A. Description/Function:	Low-Noise, High-Precision Series Voltage References
B. Process:	S45
C. Number of Device Transistors:	
D. Fabrication Location:	USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	October 31, 2012

III. Packaging Information

A. Package Type:	6-pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4190
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Jb:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	230°C/W
M. Multi Layer Theta Jc:	76°C/W

IV. Die Information

A. Dimensions:	mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 240 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 4.6 \times 10^{-9}$$

$$\lambda = 4.6 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.06 @ 25C and 1.00 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TO0ZBQ001H, D/C 1221)

The RF50 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX6071xxAUTxx+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135C	DC Parameters	80	0	TO0WBQ001J, D/C 1206
	Biased	& functionality	80	0	TO0TBQ001L, D/C 1221
	Time = 192 hrs.		80	0	TO0ZBQ001F, D/C 1221

Note 1: Life Test Data may represent plastic DIP qualification lots.