RELIABILITY REPORT
FOR
MAX5854ETL+
PLASTIC ENCAPSULATED DEVICES

May 17, 2011

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer
Conclusion

The MAX5854ETL+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX5854 dual, 10-bit, 165Msps digital-to-analog converter (DAC) provides superior dynamic performance in wideband communication systems. The device integrates two 10-bit DAC cores, and a 1.24V reference. The MAX5854 supports single-ended and differential modes of operation. The dynamic performance is maintained over the entire 2.7V to 3.6V power-supply operating range. The analog outputs support a -1.0V to +1.25V compliance voltage. The MAX5854 can operate in interleaved data mode to reduce the I/O pin count. This allows the converter to be updated on a single, 10-bit bus. The MAX5854 features digital control of channel gain matching to within ±0.4dB in sixteen 0.05dB steps. Channel matching improves sideband suppression in analog quadrature modulation applications. The on-chip 1.24V bandgap reference includes a control amplifier that allows external full-scale adjustments of both channels through a single resistor. The internal reference can be disabled and an external reference may be applied for high-accuracy applications. The MAX5854 features full-scale current outputs of 2mA to 20mA and operates from a 2.7V to 3.6V single supply. The DAC supports three modes of power-control operation: normal, low-power standby, and complete power-down. In power-down mode, the operating current is reduced to 1µA. The MAX5854 is packaged in a 40-pin thin QFN with exposed paddle (EP) and is specified for the extended (-40°C to +85°C) temperature range. Pin-compatible, lower speed, and lower resolution versions are also available. Refer to the MAX5853 (10-bit, 80Msps), the MAX5852 (8-bit, 165Msps), and the MAX5851 (8-bit, 80Msps) data sheets for more information. See Table 4 at the end of the data sheet.
II. Manufacturing Information

A. Description/Function: Dual, 10-Bit, 165Msps, Current-Output DAC
B. Process: TS35
C. Number of Device Transistors:
D. Fabrication Location: Taiwan
E. Assembly Location: China, Thailand
F. Date of Initial Production: January 23, 2004

III. Packaging Information

A. Package Type: 40-pin TQFN 6x6
B. Lead Frame: Copper
C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-9000-0844
H. Flammability Rating: Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C Level 1
J. Single Layer Theta Ja: 39°C/W
K. Single Layer Theta Jc: 2°C/W
L. Multi Layer Theta Ja: 28°C/W
M. Multi Layer Theta Jc: 2°C/W

IV. Die Information

A. Dimensions: 103 X 103 mils
B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization: None
E. Minimum Metal Width: 0.35µm
F. Minimum Metal Spacing: 0.35µm
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO₂
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (χ) is calculated as follows:

\[
\chi = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 45 \times 2}
\]

(Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

\[
\chi = 24.4 \times 10^{-9}
\]

\[
\chi = 24.4 \text{ F.I.T. (60% confidence level @ 25°C)}
\]

The following failure rate represents data collected from Maxim’s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QNB0BQ001AD/C 0346)

The CD09 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.
### Table 1
Reliability Evaluation Test Results

MAX5854ETL+

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test</td>
<td>Ta = 135°C</td>
<td>DC Parameters</td>
<td>45</td>
<td>0</td>
<td>QNB1BQ001A, D/C 0350</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.