RELIABILITY REPORT

FOR

MAX5104xEE

PLASTIC ENCAPSULATED DEVICES

October 23, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX5104 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

Table of Contents

I. Device Description
II. Manufacturing Information
III. Packaging Information
IV. Die Information
V. Quality Assurance Information
VI. Reliability Evaluation

I. Device Description

A. General

The MAX5104 low-power, serial, voltage-output, dual 12-bit digital-to-analog converter (DAC) consumes only 500µA from a single +5V supply. This device features Rail-to-Rail® output swing and is available in a space-saving 16-pin QSOP package. To maximize the dynamic range, the DAC output amplifiers are configured with an internal gain of +2V/V.

The 3-wire serial interface is SPI™/QSPI™/MICROWIRE™ compatible. Each DAC has a double-buffered input organized as an input register followed by a DAC register, which allows the input and DAC registers to be updated independently or simultaneously with a 16-bit serial word. Additional features include programmable power-down (2µA), hardware power-down lockout (PDL), a separate reference voltage input for each DAC that accepts AC and DC signals, and an active-low clear input (CL) that resets all registers and DACs to zero. These devices provide a programmable logic pin for added functionality, and a serial-data output pin for daisy chaining.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD to AGND</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>VDD to DGND</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>AGND to DGND</td>
<td>±0.3V</td>
</tr>
<tr>
<td>OSA, OSB to AGND</td>
<td>VAGND - 4V to (VDD + 0.3V)</td>
</tr>
<tr>
<td>REF+, OUT to AGND</td>
<td>-0.3V to (VDD + 0.3V)</td>
</tr>
<tr>
<td>Digital Inputs (SCLK, DIN, CS, CL, PDL) to DGND</td>
<td>(-0.3V to +6V)</td>
</tr>
<tr>
<td>Digital Outputs (DOUT, UPO) to DGND</td>
<td>-0.3V to (VDD + 0.3V)</td>
</tr>
<tr>
<td>Maximum Current into Any Pin</td>
<td>±20mA</td>
</tr>
<tr>
<td>Operating Temperature Ranges</td>
<td></td>
</tr>
<tr>
<td>MAX5104CEE</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>MAX5104EEE</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10sec)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation</td>
<td></td>
</tr>
<tr>
<td>16-Pin QSOP</td>
<td>667mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td>8.3mW/°C</td>
</tr>
<tr>
<td>16-Pin QSOP</td>
<td></td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: Low-Power, Dual, Voltage-Output, 12-Bit DAC with Serial Interface
B. Process: S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors: 3053
D. Fabrication Location: Oregon, USA
E. Assembly Location: Philippines or Thailand
F. Date of Initial Production: November, 1999

III. Packaging Information

A. Package Type: 16-Lead QSOP
B. Lead Frame: Copper
C. Lead Finish: Solder Plate
D. Die Attach: Silver-filled Epoxy
E. Bondwire: Gold (1.0 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: Buildsheet # 05-0401-0493
H. Flammability Rating: Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 86 x 114 mils
B. Passivation: Si$_3$N$_4$/SiO$_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect: Aluminum/Si (Si = 1%)
D. Backside Metallization: None
E. Minimum Metal Width: 1.2 microns (as drawn)
F. Minimum Metal Spacing: 1.2 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO$_2$
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

\[ \lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4389 \times 160 \times 2} \]  
(Chi square value for MTTF upper limit)

\[ \lambda = 14.98 \times 10^{-9} \quad \lambda = 14.98 \text{ F.I.T.} \quad \text{(60% confidence level @ 25°C)} \]

Temperature Acceleration factor assuming an activation energy of 0.8eV

This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5269) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DA65-2 die type has been found to have all pins able to withstand a transient pulse of ±2000, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.
# Table 1
Reliability Evaluation Test Results

**MAX5104xEE**

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong> (Note 1)</td>
<td>Ta = 135°C Biased Time = 192 hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td>160</td>
<td>1</td>
</tr>
<tr>
<td><strong>Moisture Testing</strong> (Note 2)</td>
<td>Pressure Pot Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td>QSOP 77</td>
<td>0</td>
</tr>
<tr>
<td>85/85</td>
<td>Ta = 85°C RH = 85% Biased Time = 1000hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong> (Note 2)</td>
<td>Temperature Cycle -65°C/150°C 1000 Cycles Method 1010</td>
<td>DC Parameters &amp; functionality</td>
<td>77</td>
<td>0</td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Each pin individually connected to terminal A with the other floating)</td>
<td>(The common combination of all like-named pins connected to terminal B)</td>
</tr>
<tr>
<td>1.</td>
<td>All pins except ( V_{PS1} ) 3/</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground
(e.g., where \( V_{PS1} \) is \( V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, +V_S, -V_S, V_{REF}, \) etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \( V_{SS1}, V_{SS2}, V_{SS3} \) or \( V_{CC1}, V_{CC2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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Mil Std 883D
Method 3015.7
Notice 8