RELIABILITY REPORT
FOR
MAX492xxA
PLASTIC ENCAPSULATED DEVICES

July 10, 2003

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by  Reviewed by
Jim Pedicord  Bryan J. Preeshl
Quality Assurance  Quality Assurance
Reliability Lab Manager  Executive Director
Conclusion

The MAX492 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The dual MAX492 operational amplifier combines excellent DC accuracy with rail-to-rail operation at the input and output. Since the common-mode voltage extends from \( V_{CC} \) to \( V_{EE} \), the device can operate from either a single supply (+2.7V to +6V) or split supplies (±1.35V to ±3V). Each op amp requires less than 150\( \mu \)A supply current. Even with this low current, the op amp is capable of driving a 1k\( \Omega \) load, and the input referred voltage noise is only 25nV/√Hz. In addition, this op amp can drive loads in excess of 1nF.

The precision performance of the MAX492, combined with its wide input and output dynamic range, low-voltage single-supply operation, and very low supply current, makes it an ideal choice for battery-operated equipment and other low-voltage applications.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (( V_{CC} ) to ( V_{EE} ))</td>
<td>7V</td>
</tr>
<tr>
<td>Common-Mode Input Voltage</td>
<td>( (V_{CC} + 0.3V) ) to ( (V_{EE} - 0.3V) )</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>±( (V_{CC} - V_{EE}) )</td>
</tr>
<tr>
<td>Input Current (IN+, IN-, NULL1, NULL2)</td>
<td>±10mA</td>
</tr>
<tr>
<td>Output Short-Circuit Duration</td>
<td>Indefinite short circuit to either supply</td>
</tr>
<tr>
<td>Voltage Applied to NULL Pins</td>
<td>( V_{CC} ) to ( V_{EE} )</td>
</tr>
<tr>
<td>Storage Temp.</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temp. (10 sec.)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td>729mW</td>
</tr>
<tr>
<td>8-Pin PDIP</td>
<td>471mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td>9.09mW/°C</td>
</tr>
<tr>
<td>8-Pin PDIP</td>
<td>5.88mW/°C</td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: Dual, Micropower, Single-Supply Rail-to-Rail Op Amp
B. Process: CBP - Complimentary Bipolar Process
C. Number of Device Transistors: 268
D. Fabrication Location: Minnesota, USA
E. Assembly Location: Philippines, Malaysia, or Thailand
F. Date of Initial Production: September, 1994

III. Packaging Information

A. Package Type: 8-Lead NSO 8-Lead PDIP
B. Lead Frame: Copper Copper
C. Lead Finish: Solder Plate Solder Plate
D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy
E. Bondwire: Gold (1.3 mil dia.) Gold (1.3 mil dia.)
F. Mold Material: Epoxy with silica filler Epoxy with silica filler
G. Assembly Diagram: # 05-0601-0391 # 05-0601-0390
H. Flammability Rating: Class UL94-V0 Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1 Level 1

IV. Die Information

A. Dimensions: 65 x 66 mils
B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect: Aluminum/Copper/Si
D. Backside Metallization: None
E. Minimum Metal Width: Metal1: 6; Metal2: 8 microns (as drawn)
F. Minimum Metal Spacing: Metal1: 2; Metal2: 3 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: $\text{SiO}_2$
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:
   Jim Pedicord (Manager, Reliability Operations)
   Bryan Preeshl (Executive Director of QA)
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

   \[
   \lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4389 \times 160 \times 2} \quad \text{(Chi square value for MTTF upper limit)}
   \]

   Temperature Acceleration factor assuming an activation energy of 0.8eV

   \[
   \lambda = 14.98 \times 10^{-9}
   \]

   \[
   \lambda = 14.98 \text{ F.I.T. (60% confidence level @ 25°C)}
   \]

   This low failure rate represents data collected from Maxim’s reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5261) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

   Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

   The OA61 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA.
### Table 1
Reliability Evaluation Test Results

#### MAX492xxA

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong> (Note 1)</td>
<td>Ta = 135°C</td>
<td>DC Parameters</td>
<td></td>
<td>160</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Moisture Testing</strong> (Note 2)</td>
<td>Ta = 121°C</td>
<td>DC Parameters</td>
<td>NSO</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Pressure Pot</td>
<td>P = 15 psi.</td>
<td>&amp; functionality</td>
<td>PDIP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>RH= 100%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 168hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>85/85</strong></td>
<td>Ta = 85°C</td>
<td>DC Parameters</td>
<td>77</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RH = 85%</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 1000hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong> (Note 2)</td>
<td>-65°C/150°C</td>
<td>DC Parameters</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Temperature Cycle</td>
<td>1000 Cycles</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Method 1010</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th></th>
<th>Terminal A (Each pin individually connected to terminal A with the other floating)</th>
<th>Terminal B (The common combination of all like-named pins connected to terminal B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>All pins except V_{PS1} 3/</td>
<td>All V_{PS1} pins</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, +V_{S}, -V_{S}, V_{REF}, etc).

3.4 Pin combinations to be tested.

- **a.** Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

- **b.** Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

- **c.** Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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**Mil Std 883D**
**Method 3015.7**
**Notice 8**