RELIABILITY REPORT
FOR
MAX485ExxA
PLASTIC ENCAPSULATED DEVICES

November 19, 2002

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

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Quality Assurance
Executive Director
Conclusion

The MAX485E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX481, MAX483, MAX485, MAX487-MAX491, and MAX1487 are low-power transceivers for RS-485 and RS-422 communication. Each part contains one driver and one receiver. The MAX483, MAX487, MAX488, and MAX489 feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 250kbps. The driver slew rates of the MAX481, MAX485, MAX490, MAX491, and MAX1487 are not limited, allowing them to transmit up to 2.5Mbps.

These transceivers draw between 120µA and 500µA of supply current when unloaded or fully loaded with disabled drivers. Additionally, the MAX481, MAX483, and MAX487 have a low-current shutdown mode in which they consume only 0.1µA. All parts operate from a single 5V supply.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX487 and MAX1487 feature quarter-unit-load receiver input impedance, allowing up to 128 MAX487/MAX1487 transceivers on the bus. Full-duplex communications are obtained using the MAX488-MAX491, while the MAX481, MAX483, MAX485, MAX487, and MAX1487 are designed for half-duplex applications.
II. Manufacturing Information

A. Description/Function: ±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceiver
B. Process: S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors: 295
D. Fabrication Location: Oregon, USA
E. Assembly Location: Malaysia, Philippines or Thailand
F. Date of Initial Production: October, 1995

III. Packaging Information

A. Package Type: 8-Lead PDIP, 8-Lead SO
B. Lead Frame: Copper, Copper
C. Lead Finish: Solder Plate, Solder Plate
D. Die Attach: Silver-filled Epoxy, Silver-filled Epoxy
E. Bondwire: Gold (1.3 mil dia.), Gold (1.3 mil dia.)
F. Mold Material: Epoxy with silica filler, Epoxy with silica filler
G. Assembly Diagram: # 05-1901-0137, # 05-1901-0136
H. Flammability Rating: Class UL94-V0, Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1, Level 1

IV. Die Information

A. Dimensions: 85 x 128 mils
B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect: Aluminum/Si (Si = 1%)
D. Backside Metallization: None
E. Minimum Metal Width: 3 microns (as drawn)
F. Minimum Metal Spacing: 3 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO₂
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
   Bryan Preeshl (Executive Director)  
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure 
   Rate ($\lambda$) is calculated as follows:

   \[
   \lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 1360 \times 2} 
   \]

   (Chi square value for MTTF upper limit)

   Temperature Acceleration factor assuming an activation energy of 0.8eV

   \[
   \lambda = 0.80 \times 10^{-9} 
   \]

   \[
   \lambda = 0.80 \text{ F.I.T. (60\% confidence level @ 25°C)} 
   \]

   This low failure rate represents data collected from Maxim’s reliability monitor program. In addition to 
   routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it 
   to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be 
   shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece 
   sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In 
   Schematic (Spec. # 06-0053) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test 
   monitors. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

   Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample 
   must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 
   85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

   The RS29 die type has been found to have all pins able to withstand a transient pulse of ±3000V, per Mil-
   Std-883 Method 3015 (reference attached ESD Test Circuit). Additionally, the MAX485E has achieved ±15kV ESD 
   protection using both methods 3015 and IEC 801-2 (air-gap discharge) on the I/O pins.

   Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.
Table 1
Reliability Evaluation Test Results
MAX485ExxE

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test (Note 1)</td>
<td>Ta = 135°C</td>
<td>DC Parameters &amp; functionality</td>
<td>1360</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Moisture Testing (Note 2)</td>
<td>Pressure Pot</td>
<td>DC Parameters &amp; functionality</td>
<td>PDIP 77</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ta = 121°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>P = 15 psi.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RH= 100%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 96hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>85/85</td>
<td>DC Parameters &amp; functionality</td>
<td>77</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ta = 85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RH = 85%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 1000hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mechanical Stress (Note 2)</td>
<td>Temperature Cycle</td>
<td>DC Parameters</td>
<td>77</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-65°C/150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1000 Cycles</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Method 1010</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data
### TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th>Terminal A (Each pin individually connected to terminal A with the other floating)</th>
<th>Terminal B (The common combination of all like-named pins connected to terminal B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. All pins except $V_{PS1}$</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2. All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination 1 for each named power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

### 3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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**Mil Std 883D**  
Method 3015.7  
Notice 8