MAX4411Exx
Rev. A

RELIABILITY REPORT

FOR

**MAX4411Exx**

PLASTIC ENCAPSULATED/CHIP SCALE DEVICES

September 30, 2003

# MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086


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**Conclusion**

The MAX4411 sucessfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

A. General

The MAX4411 fixed-gain, stereo headphone amplifier is designed for portable equipment where board space is at a premium. The MAX4411 uses a unique, patented DirectDrive architecture to produce a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors, saving cost, board space, and component height. Additionally, the gain of the amplifier is set internally (-1.5V/V, MAX4411 and -2V/V, MAX4411B), further reducing component count.

The MAX4411 delivers up to 80mW per channel into a 16Ω load and has low 0.003% THD+N. An 86dB at 217Hz power-supply rejection ratio (PSRR) allows this device to operate from noisy digital supplies without an additional linear regulator. The MAX4411 includes ±8kV ESD protection on the headphone outputs. Comprehensive click-and-pop circuitry suppresses audible clicks and pops on startup and shutdown. Independent left/right, low-power shutdown controls make it possible to optimize power savings in mixed-mode, mono/stereo applications.

The MAX4411 operates from a single 1.8V to 3.6V supply, consumes only 5mA of supply current, has short-circuit and thermal-overload protection, and is specified over the extended -40°C to +85°C temperature range. The MAX4411 is available in a tiny (2mm x 2mm x 0.6mm), 16-bump chip-scale package (UCSP™) and a 20-pin thin QFN package (4mm x 4mm x 0.8mm)

B. Absolute Maximum Rating

| Item | Rating |
|---|---|
| PGND to SGND | -0.3V to +0.3V |
| PVDD to SVDD | -0.3V to +0.3V |
| PVSS to SVSS | -0.3V to +0.3V |
| PVDD and SVDD to PGND or SGND | -0.3V to +4V |
| PVSS and SVSS to PGND or SGND | -4V to +0.3V |
| IN_ to SGND | (SVSS - 0.3V) to (SVDD + 0.3V) |
| SHDN_ to SGND | (SGND - 0.3V) to (SVDD + 0.3V) |
| OUT_ to SGND | (SVSS - 0.3V) to (SVDD +0.3V) |
| C1P to PGND | (PGND - 0.3V) to (PVDD + 0.3V) |
| C1N to PGND | (PVSS - 0.3V) to (PGND + 0.3V) |
| Output Short Circuit to GND or VDD | Continuous |
| Junction Temperature | +150°C |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Bump Temperature (soldering) Reflow | +230°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation (TA = +70°C) | |
| 16-Pin Thin QFN | 1349mW |
| 14-Bump UCSP | 589mW |
| Derates above +70°C | |
| 16-Pin Thin QFN | 16.9mW/°C |
| 14-Bump UCSP | 7.36mW/°C |

## II. Manufacturing Information

A. Description/Function: 80mW, Fixed-Gain, DirectDrive, Stereo Headphone Amplifier with Shutdown

B. Process: S8

C. Number of Device Transistors: 4295

D. Fabrication Location: California, USA

E. Assembly Location: Philippines, Thailand or Hong King

F. Date of Initial Production: October, 2002

## III. Packaging Information

| | | |
|---|---|---|
| A. Package Type: | **16-Lead QFN (4 x 4)** | **14-Bump UCSP** |
| B. Lead Frame: | Copper | N/A |
| C. Lead Finish: | Solder Plate | N/A |
| D. Die Attach: | Silver-Filled Epoxy | N/A |
| E. Bondwire: | Gold (1.0 mil dia.) | N/A |
| F. Mold Material: | Epoxy with silica filler | N/A |
| G. Assembly Diagram: | # 05-9000-0336 | # 05-9000-0122 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 | Level 1 |

## IV. Die Information

A. Dimensions: 83 x 83 mils

B. Passivation: $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Silicon

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: $SiO_2$

I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

A. Quality Assurance Contacts:

| | |
|---|---|
| Jim Pedicord | (Manager, Reliability Operations) |
| Bryan Preeshl | (Executive Director of QA) |
| Kenneth Huening | (Vice President) |

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 90 \times 2}$$ (Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 12.07 \times 10^{-9}$ $\lambda$= 12.07 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5969) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AU08-1 die type has been found to have all pins able to withstand a transient pulse of +/-1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

**Table 1**
Reliability Evaluation Test Results

**MAX4411xxE**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 90 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | uMAX<br>UCSP | 77<br>77 | 0<br>0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | uMAX<br>UCSP | 77<br>N/A | 0<br>N/A |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 (Note 3) | DC Parameters<br>& functionality | uMAX<br>UCSP | 77<br>77 | 0<br>0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: UCSP Temperature Cycle performed at -40°C/125°C, 1000 Cycles, ramp rate 11°C/minute, dwell=15 minutes, One cycle/hour

**Attachment #1**

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

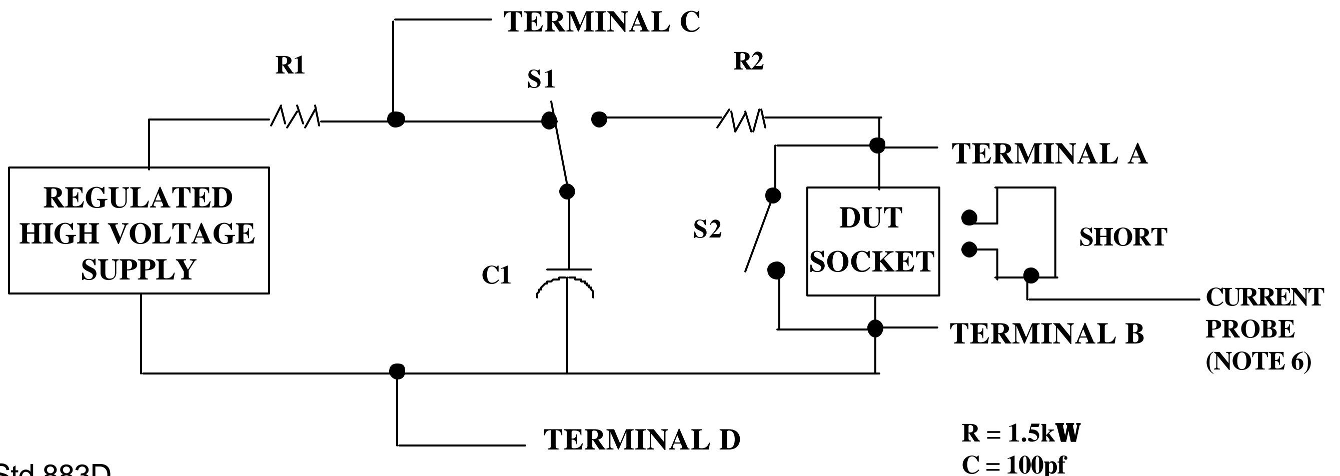
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

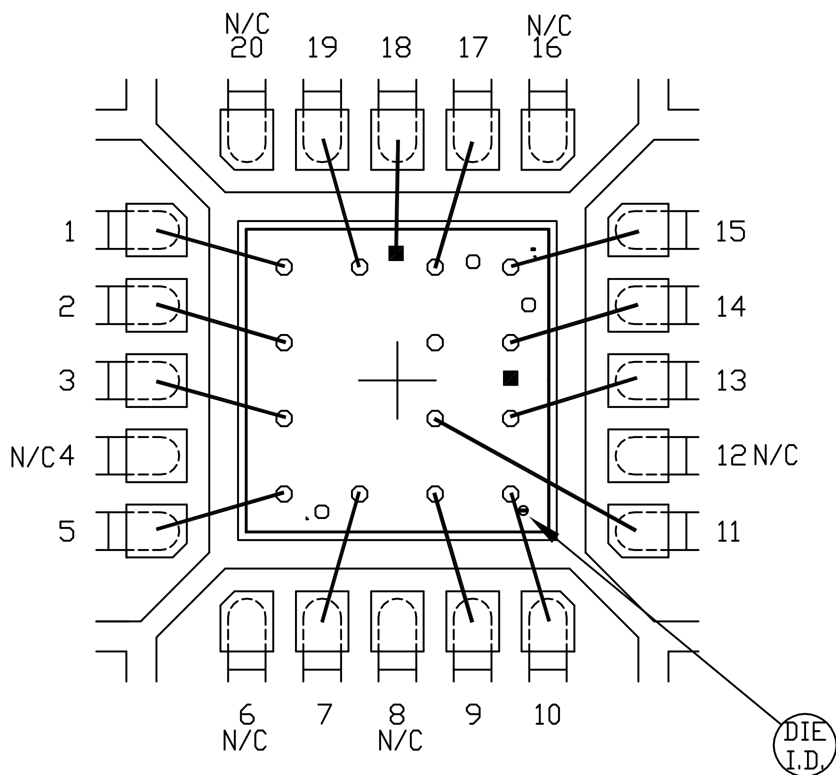
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

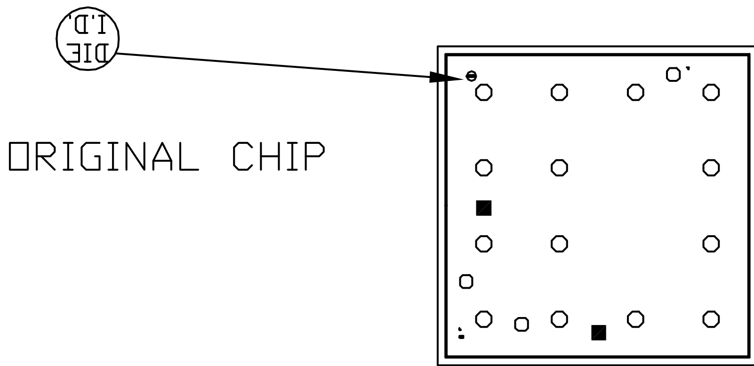
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

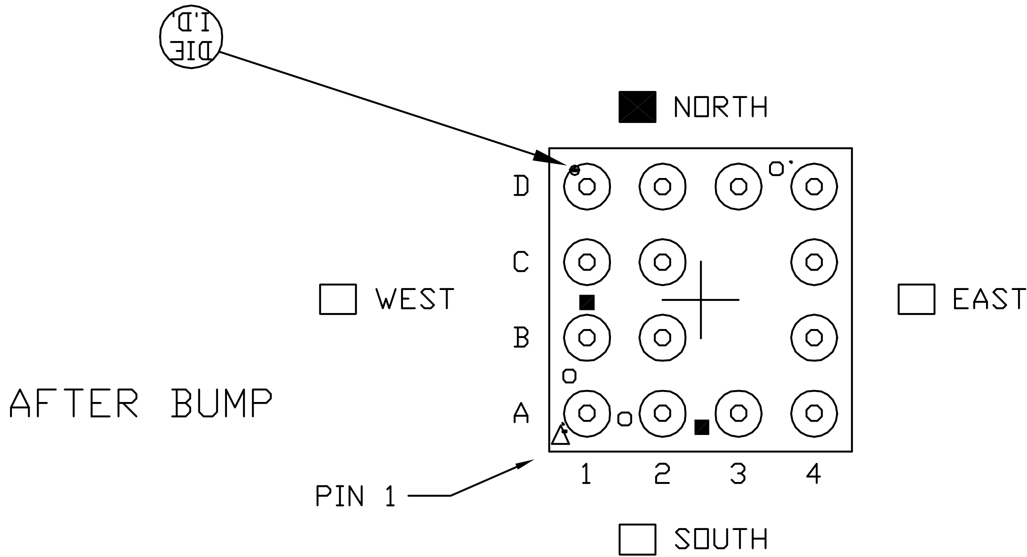


4x4x0.80mm QFN THIN PKG. EXPOSED PAD PKG.

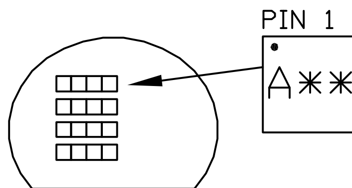


| PKG. CODE: T2044-1 | | SIGNATURES | DATE | MAXIM CONFIDENTIAL & PROPRIETARY | |
|---|---|---|---|---|---|
| CAV./PAD SIZE: 98x98 | PKG. | | | BOND DIAGRAM #: 05-9000-0336 | REV: A |
| | DESIGN | | | | |



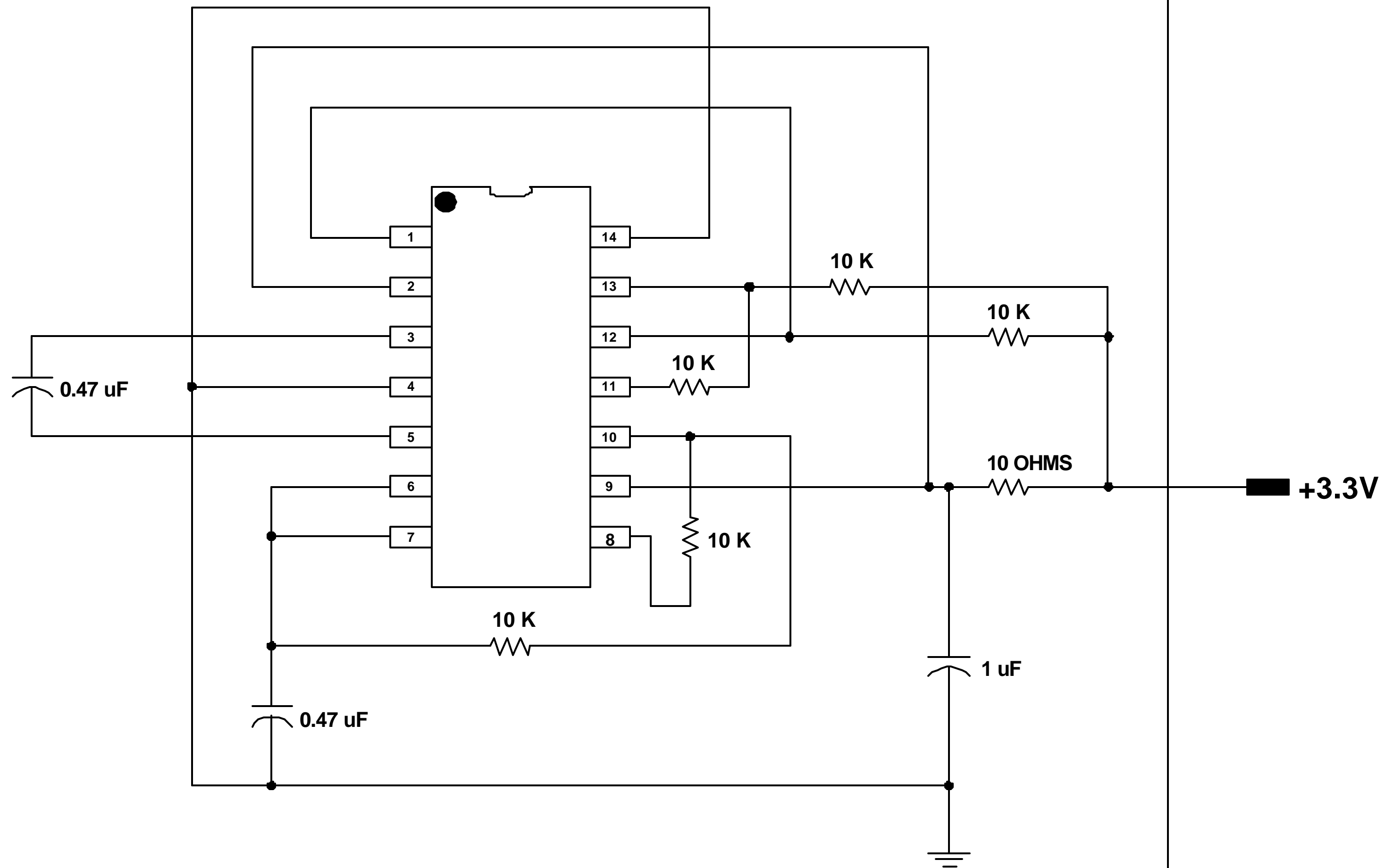




SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.




PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)

| PKG. CODE: B16-2 | | SIGNATURES | DATE | MAXIM CONFIDENTIAL & PROPRIETARY | |
|---|---|---|---|---|---|
| CAV./PAD SIZE: N/A | PKG. | | | BOND DIAGRAM #: 05-9000-0122 | REV: A |
| | DESIGN | | | | |




**DEVICES: MAX4410**
**PACKAGE: 14-TSSOP**
**MAX. EXPECTED CURRENT = 11.5 mA**

**DRAWN BY: TEK TAN**
**NOTES:**