RELIABILITY REPORT

FOR

MAX4036EXK

PLASTIC ENCAPSULATED DEVICES

July 18, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX4036 has completed qualification testing except for product level Burn-In. Package and Process qualification has been completed for the device.

Table of Contents

I. Device Description

A. General

The single MAX4036 operational amplifier operates from a single +1.4V to +3.6V (without reference) or +1.8V to +3.6V (with reference) supply and consume only 800nA of supply current per amplifier, and 1.1µA for the optional reference. The MAX4036 features a common-mode input voltage range from 0V to V_{DD} - 0.4V at V_{DD} = 1.4V.

The MAX4036's Rail-to-Rail outputs drive 5kΩ loads to within 25mV of the rails. Ultra-low supply current, low operating voltage, and rail-to-rail outputs make the MAX4036 ideal for use in singlecell lithium-ion (Li+), or two-cell NiCd/NiMH/alkaline battery-powered applications.

The MAX4036 is available in an SC70 package.

B. Absolute Maximum Ratings

Item	Rating
VDD to VSS	-0.3V to +4.0V
INA+, INB+, INA-, INB-, IN+, IN-, OUTA, OUTB, OUT, REF	(VSS - 0.3V) to (VDD + 0.3V)
OUTA, OUTB, OUT, REF Shorted to VSS or VDD	Continuous
Maximum Continuous Power Dissipation (TA = +70°C)	
5-Pin SC70 (derate 3.1mW/°C above +70°C)	247mW
6-Pin SOT23 (derate 8.7mW/°C above +70°C)	696mW
8-Pin µMAX (derate 4.5mW/°C above +70°C)	362mW
8-Pin TDFN (derate 24.4mW/°C above +70°C)	1951mW
9-Bump UCSP (derate 5.2mW/°C above +70°C)	412mW
10-Pin µMAX (derate 5.6mW/°C above +70°C)	444mW
10-Pin TDFN (derate 24.4mW/°C above +70°C)	1951mW
Operating Temperature Range	
MAX403_E_ _	-40°C to +85°C
MAX403_A_ _	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference
B. Process:	S4
C. Number of Device Transistors:	146
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines, Malaysia, Thailand, or USA
F. Date of Initial Production:	July, 2004

III. Packaging Information

A. Package Type:	**5-pin SC70**
B. Lead Frame:	Alloy 42
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0865
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	31 x 30 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1, Metal2 & Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1, Metal2 & Metal3 = 0.4 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Managing Director of QA**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.91 \times 10^{-9}$

λ = 22.91 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6278) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the S4 Process results in a FIT Rate of 0.37 @ 25C and 6.28 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The OY02 die type has been found to have all pins able to withstand a transient pulse of ±2500V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4036EXK

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SC70	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77 77	0 0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

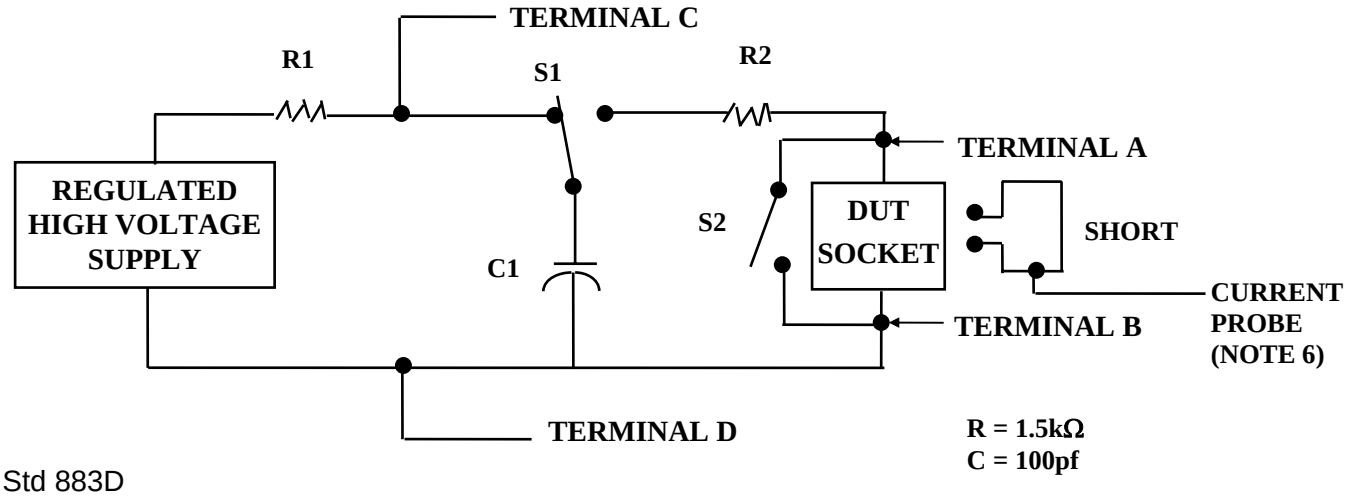
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

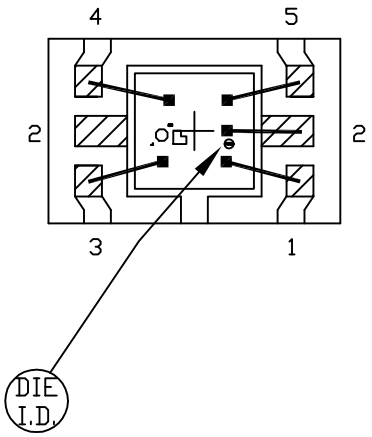
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

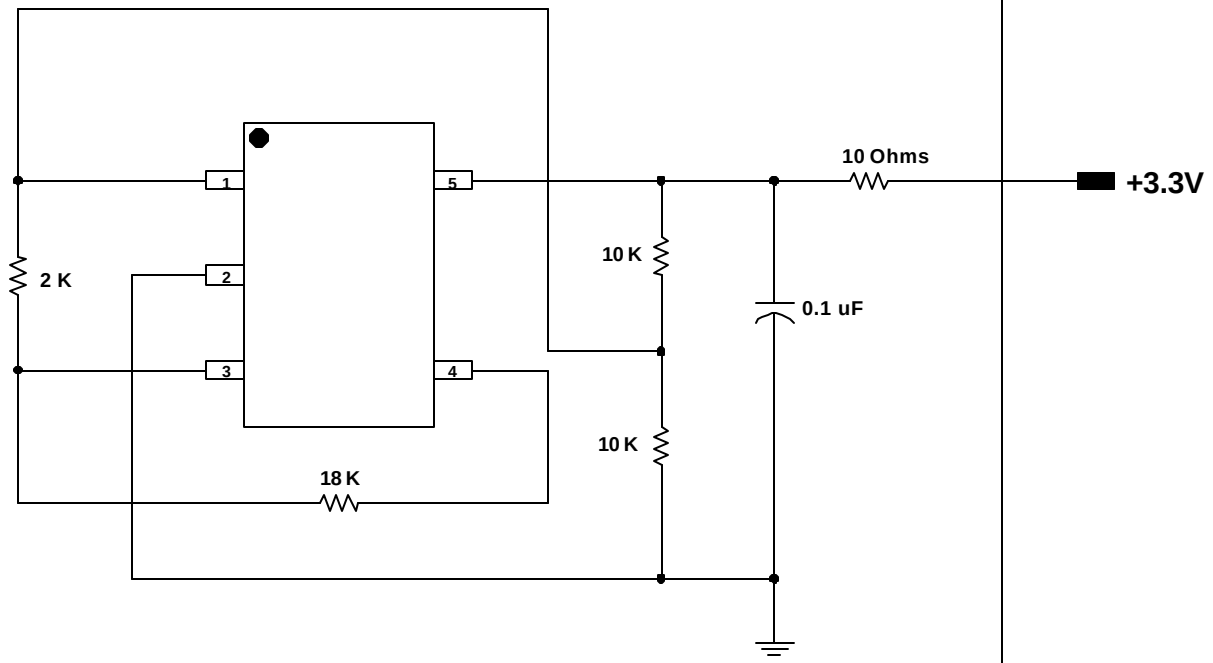




▨ BONDABLE AREA

NOTE: CAVITY DOWN

PKG. CODE: X5-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 35x34	PKG.			BOND DIAGRAM #: 05-9000-0865	REV: A
	DESIGN				

ONCE PER SOCKET	ONCE PER BOARD
	

DEVICES: MAX 4036 (OY02Z) **PACKAGE: 5-SC70** **MAX. EXPECTED CURRENT = 30uA**	**DRAWN BY: TEK TAN** **NOTES:**