MAX3804ETE
Rev. A

RELIABILITY REPORT

FOR

MAX3804ETE

PLASTIC ENCAPSULATED DEVICES

December 30, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3804 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3804 driver with integrated analog equalizer compensates up to 20dB of loss at 5GHz. It is designed to ensure PC board signal integrity up to 12.5Gbps, where frequency-dependent skin effect and dielectric losses typically produce unacceptable amounts of intersymbol interference. The MAX3804 can extend the practical chip-to-chip transmission distance for 10Gbps NRZ serial data up to 30in (0.75m) on FR-4, and it significantly decreases deterministic jitter. Residual jitter after equalization for 10.7Gbps signals is typically $24ps_{p-p}$ on the maximum path length.

The MAX3804 is ideal for 10Gbps chip-to-chip serial interconnections on inexpensive FR-4 material. Its 3mm x 3mm package affords optimal placement and routing flexibility. It has separate V_{CC} connections for internal logic and current-mode logic (CML) I/O. This allows the CML input and output to be referenced to isolated supplies, providing independent DC-coupled interfacing to 1.8V, 2.5V, or 3.3V ICs. Eight discrete levels of input equalization can be selected through a digital control input, enabling the equalizer to be matched to a range of transmission line path loss. When correctly set to match the path loss, the MAX3804 provides optimal performance over a wide range of data rates and formats.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage (VCC)	-0.5V to +4.0V
CML Supply Voltage (VCC1, VCC2)	-0.5V to (VCC + 0.5V)
Current at Serial Output (SDO+, SDO-)	+/-25mA
Input Voltage (SDI+, SDI-, EQ1, EQ2, EQ3)	-0.5V to (VCC + 0.5V)
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +150°C
Continuous Power Dissipation (TA = +85°C)	
16-Pin Thin QFN-EP	1398mW
Derates above +85°C	
16-Pin Thin QFN-EP	17.5mW/°C

II. Manufacturing Information

A. Description/Function: 12.5Gbps Settable Receive Equalizer

B. Process: GST4-F60

C. Number of Device Transistors: 1007

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia

F. Date of Initial Production: December, 2002

III. Packaging Information

A. Package Type: **16-Pin Thin QFN (3 x 3)**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: N/A

E. Bondwire: 6 mil dia. ball

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-9000-0165

H. Flammability Rating: Class: UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 84 x 84 mils

B. Passivation: Si_3N_4 (Silicon nitride)

C. Interconnect: Au

D. Backside Metallization: None

E. Minimum Metal Width: Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn)

F. Minimum Metal Spacing: Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 10.11 \times 10^{-8}$ λ = 10.11 F.I.T. (60% confidence level @ 25°C)

This bw failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-7094) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Reports (**RR-1M** & **RR-B3A**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HT31 die type has been found to have all pins able to withstand a transient pulse of +/-2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX3804ETE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

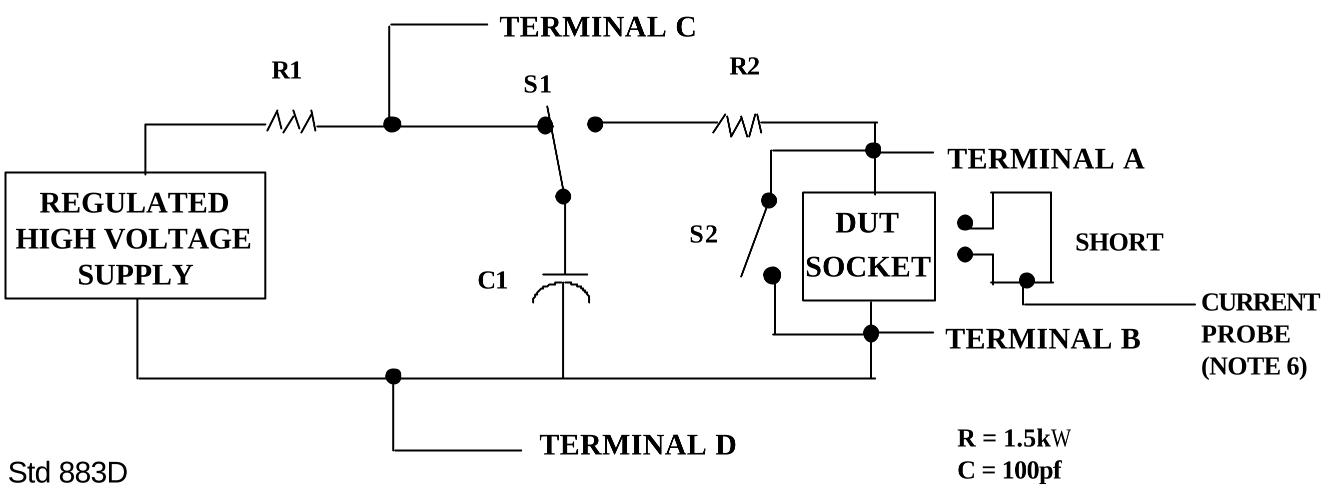
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S}$, $-V_{S}$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

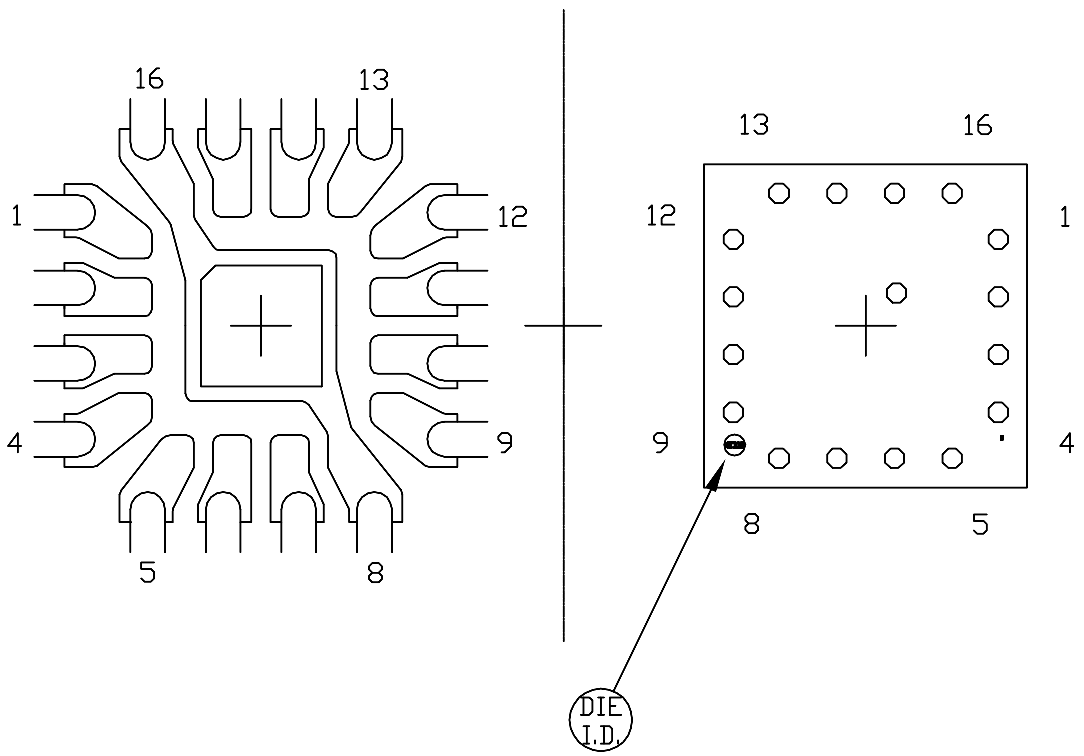
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

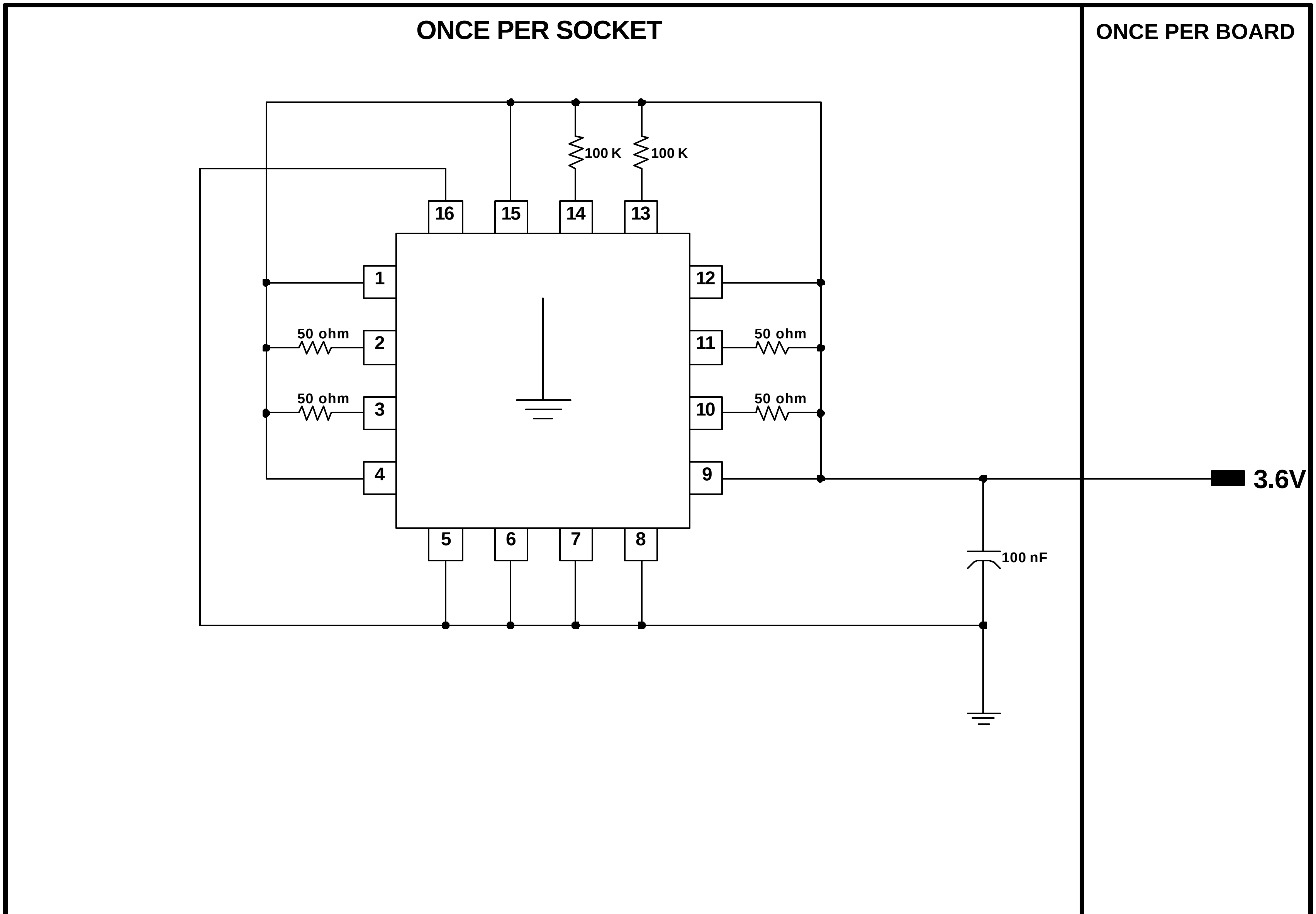


3x3x0.8mm QFN THIN PKG.
FLIP CHIP
WITH EXPOSED PAD

FLIP LINE



PKG. CODE: T1633F-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: FLIP CHIP	PKG.			BOND DIAGRAM #: 05-9000-0165	REV: A
	DESIGN				



DEVICES: MAX3804
PACKAGE: 16 - QFN (3X3-THIN)
MAX. EXPECTED CURRENT = 60mA

DRAWN BY: HAK TAN

NOTES:

DOCUMENT I.D. 06-7094	**REVISION** A	*MAXIM* **TITLE: BI Circuit (MAX3804)**	**PAGE** 2 OF 3