RELIABILITY REPORT

FOR

MAX333ACxx

PLASTIC ENCAPSULATED DEVICES

February 7, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Conclusion

The MAX333A successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX333A is a precision, quad, single-pole double-throw (SPDT) analog switch. The four independent switches operate with bipolar supplies ranging from ±4.5V to ±20V, or with a single-ended supply between +10V and +30V. The MAX333A offers low on resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the analog signal range (Δ3Ω max). It also offers break-before-make switching (10ns typical), with turn-off times less than 145ns and turn-on times less than 175ns. The MAX333A is ideal for portable operation since quiescent current runs less than 50µA with all inputs high or low.

This monolithic, quad switch is fabricated with Maxim's new improved silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), and low power consumption (3.75mW).

Logic inputs are TTL and CMOS compatible and guaranteed over a +0.8V to +2.4V range – regardless of supply voltage. Logic inputs and switched analog signals can range anywhere between the supply voltages without damage.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ to V-</td>
<td>44V</td>
</tr>
<tr>
<td>V_IN, V_COM, V_NO, V_NC</td>
<td>V- to V+</td>
</tr>
<tr>
<td>(V_NO - V_NC)</td>
<td>32V</td>
</tr>
<tr>
<td>V+ to Ground</td>
<td>30V</td>
</tr>
<tr>
<td>V- to Ground</td>
<td>-30V</td>
</tr>
<tr>
<td>Current, Any Terminal Except V_COM, V_NO, V_NC</td>
<td>30mA</td>
</tr>
<tr>
<td>Continuous Current, V_COM, V_NO, V_NC</td>
<td>20mA</td>
</tr>
<tr>
<td>Peak Current, V_COM, V_NO, V_NC</td>
<td>70mA</td>
</tr>
<tr>
<td>(Pulsed at 1ms, 10% duty cycle max)</td>
<td></td>
</tr>
<tr>
<td>Storage Temp.</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temp. (10 sec.)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td>889mW</td>
</tr>
<tr>
<td>20-Pin PDIP</td>
<td></td>
</tr>
<tr>
<td>20-Pin SO</td>
<td>800mW</td>
</tr>
<tr>
<td>20-Pin TSSOP</td>
<td>559mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td></td>
</tr>
<tr>
<td>20-Pin PDIP</td>
<td>11.11mW/^°C</td>
</tr>
<tr>
<td>20-Pin SO</td>
<td>10.0mW/^°C</td>
</tr>
<tr>
<td>20-Pin TSSOP</td>
<td>8.00mW/^°C</td>
</tr>
</tbody>
</table>

Note 1: Device mounted with all leads soldered to PC board.
II. Manufacturing Information

A. Description/Function: Precision, Quad, SPDT, CMOS Analog Switch

B. Process: S5 (SG5) - Standard 5 micron silicon gate CMOS

C. Number of Device Transistors: 145

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines, Malyasia or Thailand

F. Date of Initial Production: April, 1991

III. Packaging Information

A. Package Type: 20-Lead WSO 16-Lead PDIP 20-Lead TSSOP

B. Lead Frame: Copper Copper Copper

C. Lead Finish: Solder Plate Solder Plate Solder Plate

D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.) Gold (1.3 mil dia.) Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler Epoxy with silica filler Epoxy with silica filler

G. Assembly Diagram: # 05-0301-0614 # 05-0301-0613 # 05-0301-0869

H. Flammability Rating: Class UL94-V0 Class UL94-V0 Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1 Level 1 Level 1

IV. Die Information

A. Dimensions: 101 x 139 mils

B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 5 microns (as drawn)

F. Minimum Metal Spacing: 5 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: $\text{SiO}_2$

I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

\[
\lambda = \frac{1}{MTTF} = \frac{4.04}{192 \times 4389 \times 240 \times 2} \\
\lambda = 9.99 \times 10^{-9} \quad \text{(60% confidence level @ 25°C)}
\]

Temperature Acceleration factor assuming an activation energy of 0.8eV

This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-1742) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AG63 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.
### Table 1
Reliability Evaluation Test Results

MAX333ACxx

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong></td>
<td>Ta = 135°C</td>
<td>DC Parameters</td>
<td></td>
<td>240</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Moisture Testing</strong></td>
<td>Ta = 121°C</td>
<td>DC Parameters</td>
<td>NSO</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>P = 15 psi.</td>
<td></td>
<td>PDIP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>RH= 100%</td>
<td></td>
<td>TSSOP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Time = 168hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>85/85</strong></td>
<td>Ta = 85°C</td>
<td>DC Parameters</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>RH = 85%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 1000hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong></td>
<td>-65°C/150°C</td>
<td>DC Parameters</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1000 Cycles</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Method 1010</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th>1.</th>
<th>Terminal A (Each pin individually connected to terminal A with the other floating)</th>
<th>Terminal B (The common combination of all like-named pins connected to terminal B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where \( V_{PS1} \) is \( V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, +V_S, -V_S, V_{REF} \), etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \( V_{SS1}, V_{SS2}, V_{SS3}, V_{CC1}, V_{CC2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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Mil Std 883D
Method 3015.7
Notice 8