RELIABILITY REPORT

FOR

MAX293xxx

PLASTIC ENCAPSULATED DEVICES

January 30, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Conclusion

The MAX293 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX293 is an easy-to-use, 8th-order, lowpass, elliptic, switched-capacitor filter that can be set up with corner frequencies from 0.1Hz to 25kHz.

The MAX293’s 1.5 transition ratio provides sharp rolloff and -80dB of stopband rejection. This filter has fixed responses, so the design task is limited to selecting the clock frequency that controls the filter’s corner frequency.

An external capacitor is used to generate a clock using the internal oscillator, or an external clock signal can be used. An uncommitted op amp (noninverting input grounded) is provided for building a continuous-time lowpass filter for post-filtering or anti-aliasing. Steep rolloff and high order make this filter ideal for anti-aliasing applications that require maximum bandwidth and communication applications that require filtering signals in close proximity within the frequency domain.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V+ to V-)</td>
<td>12V</td>
</tr>
<tr>
<td>Input Voltage at Any Pin</td>
<td>(V- -0.3V) V\text{IN} (V+ +0.3V)</td>
</tr>
<tr>
<td>Storage Temp.</td>
<td>-65°C to +160°C</td>
</tr>
<tr>
<td>Lead Temp. (10 sec.)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td>762mW</td>
</tr>
<tr>
<td>16-Pin WSO</td>
<td>727mW</td>
</tr>
<tr>
<td>8-Pin PDIP</td>
<td></td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td>9.52mW/°C</td>
</tr>
<tr>
<td>16-Pin WSO</td>
<td>9.09mW/°C</td>
</tr>
<tr>
<td>8-Pin PDIP</td>
<td></td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: 8th-Order, Lowpass, Elliptic, Switch-Capacitor Filter
B. Process: S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors: 620
D. Fabrication Location: Oregon, USA
E. Assembly Location: Philippines, Malaysia, or Thailand
F. Date of Initial Production: May, 1992

III. Packaging Information

A. Package Type: 8-Lead PDIP 16-Lead WSO
B. Lead Frame: Copper Copper
C. Lead Finish: Solder Plate Solder Plate
D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy
E. Bondwire: Gold (1.3 mil dia.) Gold (1.3 mil dia.)
F. Mold Material: Epoxy with silica filler Epoxy with silica filler
G. Assembly Diagram: # 05-0201-0111 # 05-0201-0113
H. Flammability Rating: Class UL94-V0 Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1 Level 1

IV. Die Information

A. Dimensions: 89 x 95 mils
B. Passivation: Si$_3$N$_4$/SiO$_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect: Aluminum/Si (Si = 1%)
D. Backside Metallization: None
E. Minimum Metal Width: 3 microns (as drawn)
F. Minimum Metal Spacing: 3 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO$_2$
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contact: Jim Pedicord (Manager, Rel Operations)
   Bryan Preeshl (Executive Director of QA)
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

   $\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 560 \times 2}$

   (Chi square value for MTTF upper limit)

   $\lambda = 1.94 \times 10^{-9}$

   Temperature Acceleration factor assuming an activation energy of 0.8eV

   $\lambda = 1.94 \text{ F.I.T. (60% confidence level @ 25°C)}$

   This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-4086) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

   Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

   The AF11-4 die type has been found to have all pins able to withstand a transient pulse of 1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±200mA.
Table 1

Reliability Evaluation Test Results

MAX293xxx

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test (Note 1)</strong></td>
<td>Ta = 135°C Biased</td>
<td>DC Parameters &amp; functionality</td>
<td>WSO</td>
<td>560</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Moisture Testing (Note 2)</strong></td>
<td>Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td>WSO</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Pressure Pot</td>
<td>Ta = 85°C RH = 85% Biased</td>
<td>DC Parameters &amp; functionality</td>
<td>PDIP</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Time = 1000hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Mechanical Stress (Note 2)</strong></td>
<td>Ta = -65°C/150°C 1000 Cycles Method 1010</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Package/Process data
### Attachment #1

**TABLE II.** Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th></th>
<th>Terminal A (Each pin individually connected to terminal A with the other floating)</th>
<th>Terminal B (The common combination of all like-named pins connected to terminal B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

### 3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.