RELIABILITY REPORT

FOR

MAX2391EGI

PLASTIC ENCAPSULATED DEVICES

February 3, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Quality Assurance
Executive Director
Conclusion

The MAX2391 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX2391 fully integrated direct-conversion receiver IC is designed specifically for W-CDMA applications. With the MAX2395, the MAX2391 forms a complete single-mode W-CDMA radio chipset.

The MAX2391 provides a complete antenna-to-baseband solution for the 3GPP W-CDMA FDD receiver (2110MHz to 2170MHz, 3.84Mcps), eliminating the use of an off-chip IF SAW filter, as well as external RX LO generation and synthesis.

The MAX2391 receiver ICs have over 90dB of dynamic gain control, and a receive sensitivity of -112dBm referred to LNA input. The receiver consists of an ultra-low current low-noise amplifier (LNA) with on-chip output matching and a two-step gain control. The zero-IF demodulator has a differential circuit topology for minimum LO leakage to the receiver’s input. The channel selectivity is done completely in the baseband section of the receiver with an on-chip lowpass filter. The AGC section has over 50dB of gain control range. LO quadrature generation is done onchip through a divide-by-2 prescaler. The DC offset cancellation in the I/Q baseband channels is done fully on-chip using a DC servo loop. To quickly correct for large DC offset transients in minimal time, very fast settling time is obtained by optimization of the DC-offset cancellation circuit’s time constant.

The MAX2391 includes a 3-wire serial bus for PLL programming and for configuring the different receiver modes. It also includes a SHDN pin for full device shutdown. The MAX23911s fabricated using an advanced high-frequency SiGe BiCMOS process. The IC operates from a single +2.7V to +3.3V supply and is housed in a small 28-pin leadless QFN-EP package (5mm × 5mm).

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC to GND</td>
<td>-0.3V to +3.6V</td>
</tr>
<tr>
<td>All Other Pins to GND</td>
<td>-0.3V to (VCC + 0.3V)</td>
</tr>
<tr>
<td>LNA_IN</td>
<td>+15dBm</td>
</tr>
<tr>
<td>Digital Input Current</td>
<td>±10mA</td>
</tr>
<tr>
<td>Digital Output Open-Collector Current</td>
<td>1mA</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +160°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>28-Pin QFN</td>
<td>1.667W</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td>20.8mW/°C</td>
</tr>
<tr>
<td>28-Pin QFN</td>
<td></td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: W-CDMA Zero-IF Receivers
B. Process: MB20 Bi-CMOS Process
C. Number of Device Transistors: 8883
D. Fabrication Location: Oregon, USA
E. Assembly Location: Korea
F. Date of Initial Production: January, 2003

III. Packaging Information

A. Package Type: 28-Pin QFN
B. Lead Frame: Copper
C. Lead Finish: Solder Plate
D. Die Attach: Silver-Filled Epoxy
E. Bondwire: Gold (1.0 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: # 05-9000-1020
H. Flammability Rating: Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 120 x 98 mils
B. Passivation: Si$_3$N$_4$ (Silicon nitride)
C. Interconnect: Au
D. Backside Metallization: None
E. Minimum Metal Width: 1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing: 1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions: 3.4 mil. Octagonal
H. Isolation Dielectric: SiO$_2$
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:  Jim Pedicord (Manager, Reliability Operations)  
                              Bryan Preeshl (Executive Director of QA)   
                              Kenneth Huening (Vice President)  

B. Outgoing Inspection Level:  0.1% for all electrical parameters guaranteed by the Datasheet.  
                                0.1% For all Visual Defects. 

C. Observed Outgoing Defect Rate:  < 50 ppm 

D. Sampling Plan:  Mil-Std-105D 

VI. Reliability Evaluation 

A. Accelerated Life Test 

   The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows: 

   \[ \lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 99 \times 2} \) (Chi square value for MTTF upper limit) 

   Temperature Acceleration factor assuming an activation energy of 0.8eV 

   \[ \lambda = 4.90 \times 10^{-9} \] \[ \lambda = 4.90 \text{ F.I.T.} \text{ (60% confidence level @ 25°C)} \] 

   This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic #06-7084 shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-B2A). 

B. Moisture Resistance Tests 

   Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family. 

C. E.S.D. and Latch-Up Testing 

   The WC17-1 die type has been found to have all pins able to withstand a transient pulse of <200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.
## Table 1
Reliability Evaluation Test Results

**MAX2391EGI**

<table>
<thead>
<tr>
<th>Test Item</th>
<th>Test Condition</th>
<th>Failure Identification</th>
<th>Sample Size</th>
<th>Number of Failures</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test (Note 1)</td>
<td>$T_a = 150^\circ C$</td>
<td>DC Parameters</td>
<td>99</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Moisture Testing (Note 2)</td>
<td>Pressure Pot $T_a = 121^\circ C$</td>
<td>DC Parameters</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>$P = 15$ psi.</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$RH = 100%$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 168 hrs.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>85/85</td>
<td>DC Parameters</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>$T_a = 85^\circ C$</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$RH = 85%$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 1000 hrs.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mechanical Stress (Note 2)</td>
<td>Temperature Cycle $-65^\circ C$/</td>
<td>DC Parameters</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>$150^\circ C$</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Cycle 1000 Cycles Method 1010</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification packages.
Note 2: Generic package/process data.
### TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th>Terminal A (Each pin individually connected to terminal A with the other floating)</th>
<th>Terminal B (The common combination of all like-named pins connected to terminal B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. All pins except $V_{PS1}$, 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2. All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_{S}$, $-V_{S}$, $V_{REF}$, etc).

#### 3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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**REGULATED HIGH VOLTAGE SUPPLY**

**TERMINAL C**

**TERMINAL A**

**TERMINAL B**

**TERMINAL D**

R = 1.5kΩ  
C = 100pf

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Mil Std 883D  
Method 3015.7  
Notice 8
BONDABLE AREA

PKG. BODY SIZE: 5x5 mm

PKG. CODE: G2855-2

CAV./PAD SIZE: 130x130

SIGNATURES

PKG.

DESIGN

DATE

BOND DIAGRAM #: 05-9000-1020

REV: A

DOWNBOND DETAILS:
DOWNBOND LENGTHS ARE CRITICAL.
CONTROL DOWNBOND LOCATIONS AS SHOWN.

0.00 (DIE EDGE)
15 MILS MIN
25 MILS MAX