RELIABILITY REPORT
FOR
MAX1957EUB
PLASTIC ENCAPSULATED DEVICES

October 29, 2002

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

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Executive Director
Conclusion

The MAX1957 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1957 is a versatile, economical, synchronous current-mode, pulse-width modulation (PWM) buck controllers. This step-down controller is targeted for applications where cost and size are critical.

The MAX1957 operates at a fixed 1MHz switching frequency, thus significantly reducing external component size and cost. Additionally, excellent transient response is obtained using less output capacitance.

The MAX1957 features a tracking output voltage range of 0.4V to 0.86V<sub>IN</sub> and is capable of sourcing or sinking current for applications such as DDR bus termination and PowerPC™/ASIC/DSP core supplies. The MAX1957 operates from a 3V to 5.5V input voltage and at a fixed 300kHz switching frequency.

The MAX1957 provides a COMP pin that can be pulled low to shut down the converter in addition to providing compensation to the error amplifier. An input undervoltage lockout (ULVO) is provided to ensure proper operation under power-sag conditions to prevent the external power MOSFETs from overheating. Internal digital soft-start is included to reduce inrush current. The MAX1957 is available in tiny 10-pin µMAX packages.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN, FB to GND</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>LX to BST</td>
<td>-6V to +0.3V</td>
</tr>
<tr>
<td>BST to GND</td>
<td>-0.3V to +20V</td>
</tr>
<tr>
<td>DH to LX</td>
<td>-0.3V to (VBST + 0.3V)</td>
</tr>
<tr>
<td>DL, COMP to GND</td>
<td>-0.3V to (VIN + 0.3V)</td>
</tr>
<tr>
<td>HSD, ILIM, REFIN to GND</td>
<td>-0.3V to 14V</td>
</tr>
<tr>
<td>PGND to GND</td>
<td>-0.3V to +0.3V</td>
</tr>
<tr>
<td>IDH, IDL</td>
<td>±100mA (RMS)</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td>444mW</td>
</tr>
<tr>
<td>10-Pin µMAX</td>
<td></td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td></td>
</tr>
<tr>
<td>10-Pin µMAX</td>
<td>5.6mW/°C</td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: Low-Cost, High-Frequency, Current-Mode PWM Buck Controller
B. Process: S8 - Standard 8 micron silicon gate CMOS
C. Number of Device Transistors: 2930
D. Fabrication Location: California, USA
E. Assembly Location: Philippines, Malaysia or Thailand
F. Date of Initial Production: April, 2002

III. Packaging Information

A. Package Type: 10-Lead uMAX
B. Lead Frame: Copper
C. Lead Finish: Solder Plate
D. Die Attach: Silver-filled Epoxy
E. Bondwire: Gold (1.3 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: Buildsheet # 05-3501-0028
H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 62 X 82 mils
B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect: TiW/ AlCu/ TiWN
D. Backside Metallization: None
E. Minimum Metal Width: .8 microns (as drawn)
F. Minimum Metal Spacing: .8 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO₂
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
   Bryan Preeshl (Executive Director of QA)
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

   \[
   \lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 44 \times 2} \quad (\text{Chi square value for MTTF upper limit})
   \]

   \[
   = \frac{1}{192 \times 4389 \times 44 \times 2} \quad \text{Temperature Acceleration factor assuming an activation energy of 0.8eV}
   \]

   \[
   \lambda = 24.68 \times 10^{-9} \quad \lambda = 24.68 \text{ F.I.T. (60% confidence level @ 25°C)}
   \]

   This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-6012) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M) located on the Maxim website at http://www.maxim-ic.com.

B. Moisture Resistance Tests

   Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

   The PM42-2 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.
Table 1
Reliability Evaluation Test Results

MAX1957EUB

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong> (Note 1)</td>
<td>Ta = 135°C biased</td>
<td>DC Parameters &amp; functionality</td>
<td>44</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Moisture Testing</strong> (Note 2)</td>
<td>Pressure Pot  Ta = 121°C</td>
<td>DC Parameters &amp; functionality</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>P = 15 psi.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RH= 100%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 168hrs.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>85/85</td>
<td>DC Parameters &amp; functionality</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Ta = 85°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RH = 85%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 1000hrs.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong> (Note 2)</td>
<td>Temperature Cycle -65°C/150°C</td>
<td>DC Parameters</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1000 Cycles</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Method 1010</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th></th>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(Each pin individually connected to terminal A with the other floating)</td>
<td>(The common combination of all like-named pins connected to terminal B)</td>
</tr>
<tr>
<td>1.</td>
<td>All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.
DEVICES: MAX 1953/54/57
PACKAGE: 10-uMAX
MAX. EXPECTED CURRENT = 8mA (20V), 2mA (5V).

NOTES:

ONCE PER SOCKET

ONCE PER BOARD

DRAWN BY: TEK / HAK TAN