RELIABILITY REPORT

FOR

MAX1926ETC

PLASTIC ENCAPSULATED DEVICES

July 11, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX1926 sucessfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1926 single-cell lithium-ion (Li+) switch-mode battery charger uses an external PMOS pass element step-down configuration. Charge current is programmable, and an external capacitor sets the maximum charge time.

Additional features include automatic input power detection (ACON-bar output), logic-controlled enable, and temperature monitoring with an external thermistor. The MAX1925 disables charging for inputs greater than 6.1V.

The MAX1926 features two precondition levels to restore near-dead cells. The device sources 4mA to a cell that is below 2V while sourcing C/10 to a cell between 2V and 3V. Full charge current is then applied above 3V. A CHG-bar output drives an LED to indicate charging (LED on) and fault conditions (LED blinking).

The MAX1926 is available in a 12-pin 4mm x 4mm thin QFN package and is specified over the extended temperature range (-40°C to +85°C).

B. Absolute Maximum Ratings

Item	Rating
IN, INP, ACON to GND	-0.3V to +14V
CHG, EXT to PGND	-0.3V to (VINP + 0.3V)
CS, BATT, EN, THRM to GND	-0.3V to +6V
CT to GND	-0.3V to +4V
EN, THRM, CT to IN	-14V to +0.3V
INP to IN	-0.3V to +0.3V
PGND to GND	-0.3V to +0.3V
CS to BATT	-0.3V to +0.3V
EXT Continuous RMS Current	±100mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
Exposed Paddle Soldered to Board	
12-Pin QFN	1349mW
Exposed Paddle Unsoldered	
12-Pin QFN	721mW
Derates above +70°C	
Exposed Paddle Soldered to Board	
12-Pin QFN	16.9mW/°C
Exposed Paddle unsoldered	
12-Pin QFN	9.0mW/°C

II. Manufacturing Information

A. Description/Function:	Switch-Mode 1-Cell Li+ Chargers
B. Process:	B8 (Standard .8 micron Silicon gate CMOS)
C. Number of Device Transistors:	5722
D. Fabrication Location:	California, USA
E. Assembly Location:	Thailand or Hong Kong
F. Date of Initial Production:	July , 2002

III. Packaging Information

A. Package Type:	**12-Pin QFN (4x4)**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-3501-0032
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	81 x 81 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliablity Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 22.62 \times 10^{-9}$ $\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5989) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PM40-1 die type has been found to have all pins able to withstand a transient pulse of 600V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1926ETC

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

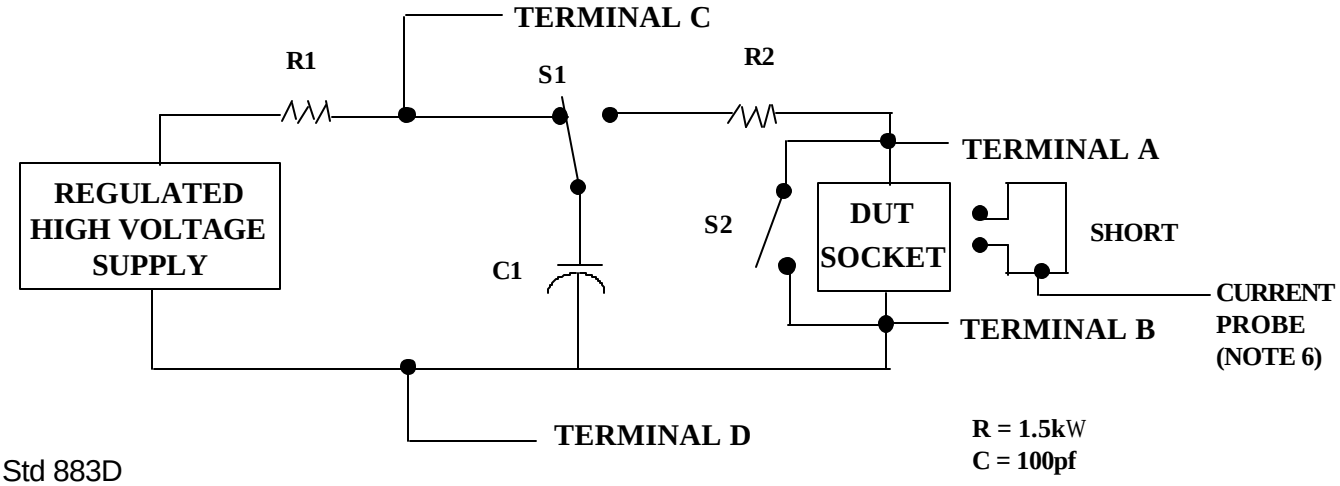
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

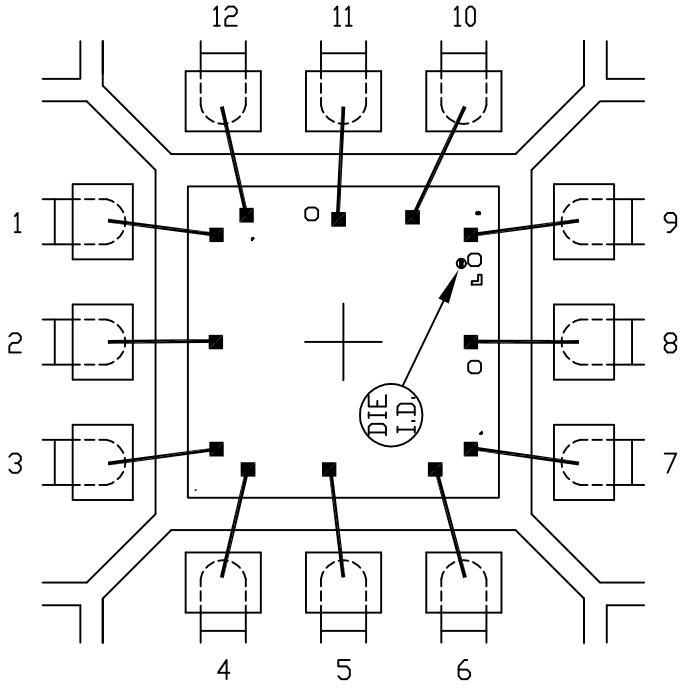
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



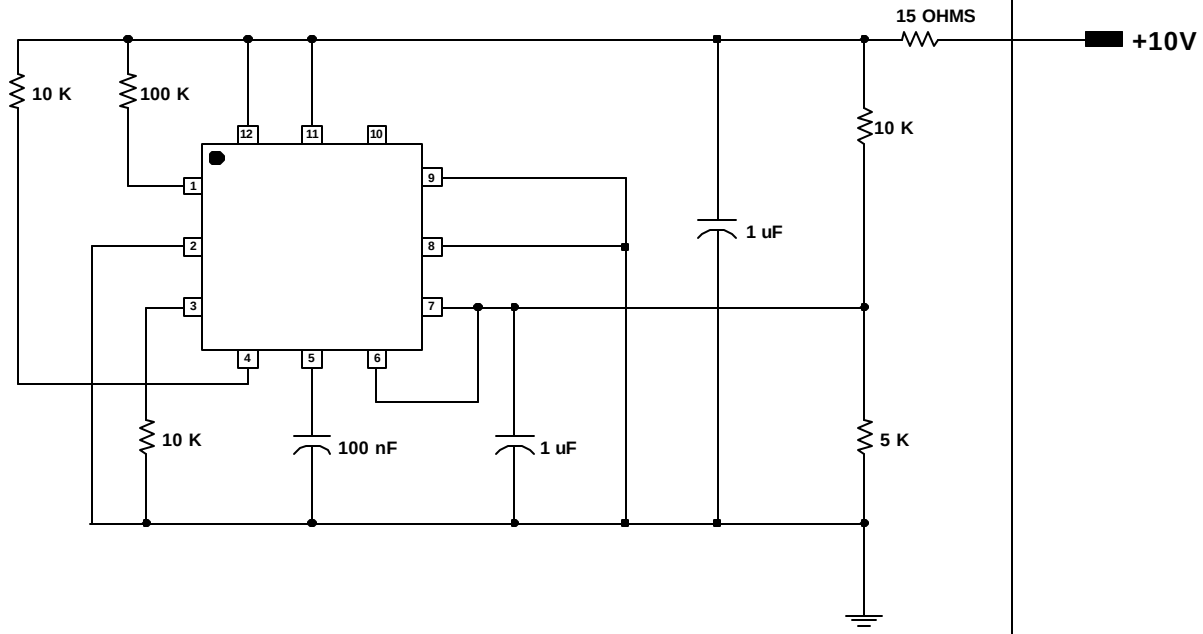
4x4x0.8 MM QFN THIN PKG. EXPOSED PAD PKG.



PKG. CODE: T1244-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 98x98	PKG.			BOND DIAGRAM #: 05-3501-0032	REV: B
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 1925/1926
PACKAGE: 12-QFN (4x4mm-THIN)
MAX. EXPECTED CURRENT = 8mA

DRAWN BY: TEK TAN
NOTES: