RELIABILITY REPORT

FOR

MAX1889ETE

PLASTIC ENCAPSULATED DEVICES

April 4, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Conclusion

The MAX1889 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

The MAX1889 provides the three regulated output voltages required for active matrix, thin-film transistor liquid crystal displays (TFT LCDs). It combines a high-performance step-up regulator with two linear-regulator controllers and multiple levels of protection circuitry for a complete power-supply system.

The main DC-DC converter is a high-frequency (500kHz/1MHz), current-mode step-up regulator with an integrated N-channel power MOSFET that allows the use of ultra-small inductors and ceramic capacitors. With its high closed-loop bandwidth performance, the MAX1889 provides fast transient response to pulsed loads while operating with efficiencies over 85%. The positive and negative linear-regulator controllers post-regulate charge-pump outputs for TFT gate-on and gate-off supplies.

The MAX1889 has a unique input switch control that can replace the typical input fuse by disconnecting the load from the input supply when a fault is detected. The fault detector monitors all three regulated output voltages and can monitor current from the input supply as well. Additionally, the MAX1889 enters thermal shutdown when its overtemperature threshold is reached.

The MAX1889 undervoltage lockout is set at 2.5V (max) to allow the input supply to droop under pulsed load conditions while avoiding any unexpected behavior when its input voltage dips momentarily. Also, the built-in soft-start and cycle-by-cycle current limiting prevent input surge currents during power-up.

The MAX1889 is available in a 16-pin thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panel design.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN, SHDN, OCN, OCP, FB, FBP, FBN, FREQ to GND</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>PGND to GND</td>
<td>±0.3V</td>
</tr>
<tr>
<td>LX to PGND</td>
<td>-0.3V to +14V</td>
</tr>
<tr>
<td>DRVP to GND</td>
<td>-0.3V to +30V</td>
</tr>
<tr>
<td>REF, GATE, TGNd to GND</td>
<td>-0.3V to (VIN + 0.3V)</td>
</tr>
<tr>
<td>DRVN to GND</td>
<td>(VIN - 28V) to (VIN + 0.3V)</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C) 16-Pin QFN</td>
<td>1538mW</td>
</tr>
<tr>
<td>Derates above +70°C 16-Pin QFN</td>
<td>19.2mW/°C</td>
</tr>
</tbody>
</table>

Continuous Power Dissipation (TA = +70°C)
II. Manufacturing Information

A. Description/Function: Quick-PWM Step-Down Controller with Inductor Saturation Protection and Dynamic Output Voltages

B. Process: B8 (Standard 0.8 micron silicon gate CMOS)

C. Number of Device Transistors: 2616

D. Fabrication Location: California, USA

E. Assembly Location: Thailand or Hong Kong

F. Date of Initial Production: July, 2002

III. Packaging Information

A. Package Type: 16-Lead Thin QFN (5 x 5)

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled epoxy

E. Bondwire: Gold (1.3 mil dia)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-9000-0349

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity
   Per JEDEC standard J-STD-020-A: Level 1

IV. Die Information

A. Dimensions: 84 x 92 mils

B. Passivation: \( \text{Si}_3\text{N}_4/\text{SiO}_2 \) (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Silicon

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: \( \text{SiO}_2 \)

I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:
   Jim Pedicord (Manager, Reliability Operations)
   Bryan Preeshl (Executive Director of QA)
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For All Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in *Table 1*. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

   $$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 44 \times 2}$$

   Thermal acceleration factor assuming a 0.8eV activation energy

   $$\lambda = 2.468 \times 10^{-9} \quad \lambda = 24.68 \text{ F.I.T. (60% confidence level @ 25°C)}$$

   This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5909) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (*RR-1M*).

B. Moisture Resistance Tests

   Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

   The PD05 die type has been found to have all pins able to withstand a transient pulse of ±200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.
## Table 1
Reliability Evaluation Test Results

**MAX1889ETE**

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test (Note 1)</td>
<td>Ta = 135°C Biased Time = 192 hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>44</td>
<td>0</td>
</tr>
<tr>
<td>Moisture Testing (Note 2)</td>
<td>Pressure Pot Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td>QFN</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>85/85 Ta = 85°C RH = 85% Biased Time = 1000hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Mechanical Stress (Note 2)</td>
<td>Temperature Cycle -65°C/150°C 1000 Cycles Method 1010</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th></th>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(Each pin individually connected to terminal A with the other floating)</td>
<td>(The common combination of all like-named pins connected to terminal B)</td>
</tr>
<tr>
<td>1.</td>
<td>All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.
DEVICES: MAX 1889
PACKAGE: 16-QFN (5x5mm body)
MAX. EXPECTED CURRENT = 12mA (+5V), 22mA (+10V).