RELIABILITY REPORT
FOR
MAX1846EUB
PLASTIC ENCAPSULATED DEVICES

April 28, 2003

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

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Reviewed by
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Quality Assurance
Executive Director
Conclusion

The MAX1846 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

MAX1846 high-efficiency PWM inverting controller allows designers to implement compact, low-noise, negative-output DC-DC converters for telecom and networking applications. The device operates from a +3V to +16.5V input and generates -2V to -200V output. To minimize switching noise, the device features a current-mode, constant-frequency PWM control scheme. The operating frequency can be set from 100kHz to 500kHz through a resistor.

The MAX1846 is available in an ultra-compact 10-pin µMAX package. Operation at high frequency, compatibility with ceramic capacitors, and inverting topology without transformers allow for a compact design. Compatibility with electrolytic capacitors and flexibility to operate down to 100kHz allow users to minimize the cost of external components. The high-current output drivers are designed to drive a P-channel MOSFET and allow the converter to deliver up to 30W.

Current-mode control simplifies compensation and provides good transient response. Accurate current-mode control and over current protection are achieved through low-side current sensing.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN, SHDN to GND</td>
<td>-0.3V to +20V</td>
</tr>
<tr>
<td>PGND to GND</td>
<td>-0.3V to +0.3V</td>
</tr>
<tr>
<td>VL to PGND for VIN = 5.7V</td>
<td>-0.3V to (VIN + 0.3V)</td>
</tr>
<tr>
<td>VL to PGND for VIN &gt; 5.7V</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>EXT to PGND</td>
<td>-0.3V to (VIN + 0.3V)</td>
</tr>
<tr>
<td>REF, COMP to GND</td>
<td>-0.3V to (VL + 0.3V)</td>
</tr>
<tr>
<td>CS, FB, FREQ, POL, SYNC to GND</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td>444mW</td>
</tr>
<tr>
<td>10-Pin µMAX</td>
<td>5.6mW/°C</td>
</tr>
</tbody>
</table>

Derates above +70°C
II. Manufacturing Information

A. Description/Function: High-Efficiency, Current-Mode, Inverting PWM Controller

B. Process: B8

C. Number of Device Transistors: 2441

D. Fabrication Location: California, USA

E. Assembly Location: Philippines, Malaysia or Thailand

F. Date of Initial Production: July, 2001

III. Packaging Information

A. Package Type: 10-Lead µMAX

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-2301-0116

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity
   Per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 62 x 87 mils

B. Passivation: Si$_3$N$_4$/SiO$_2$ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Silicon

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO$_2$

I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:
   Jim Pedicord  (Reliability Lab Manager)
   Bryan Preeshl  (Executive Director of QA)
   Kenneth Huening  (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

   0.1% For All Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

   $\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$

   (Chi square value for MTTF upper limit)

   Thermal acceleration factor assuming a 0.8eV activation energy

   $\lambda = 13.57 \times 10^{-9}$  \(\lambda = 13.57\) F.I.T. (60% confidence level @ 25°C)

   This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5860) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

   Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

   The PY85 die type has been found to have all pins able to withstand a transient pulse of $\pm 600\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.
# Table 1
Reliability Evaluation Test Results

MAX1846EUB

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test</td>
<td>( T_a = 135^\circ C )</td>
<td>DC Parameters &amp; functionality</td>
<td>80</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Moisture Testing</td>
<td>( P = 15 \text{ psi} )</td>
<td>DC Parameters &amp; functionality</td>
<td>uMAX</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td>Pressure Pot</td>
<td>( T_a = 121^\circ C )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RH = 100%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 168 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>85/85</td>
<td>( T_a = 85^\circ C )</td>
<td>DC Parameters &amp; functionality</td>
<td>77</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RH = 85%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 1000 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mechanical Stress</td>
<td>(-65^\circ C/150^\circ C)</td>
<td>DC Parameters</td>
<td>77</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Cycle</td>
<td>1000 Cycles</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data
### Table II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th>Terminal A (Each pin individually connected to terminal A with the other floating)</th>
<th>Terminal B (The common combination of all like-named pins connected to terminal B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2. All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

### 3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$ or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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[Diagram of REGULATED HIGH VOLTAGE SUPPLY, TERMINAL A, TERMINAL B, TERMINAL C, TERMINAL D, DUT SOCKET, CURRENT PROBE (NOTE 6), S1, S2, R1, R2, C1, C2, R = 1.5kΩ, C = 100pf]
DEVICES: MAX 1847EEE
MAX. EXPECTED CURRENT =  10 mA

NOTES:

ONCE PER SOCKET

ONCE PER BOARD

DRAWN BY: Iuliana Tanase

GROUND

15 V

1 uF

0.1 uF

140K

1 uF

16-QSOPI

1 2 3 4 5 6 7 8

1 POL SYNC 16

2 VL V+ 15

3 FREQ EXT 14

4 COMP CS 13

5 REF PGND 12

6 FB GND 11

7 NC GND 10

8 SHDNB NC 9

16-QSOPI

GROUND

15 V

1 uF

0.1 uF

140K

1 uF

16-QSOPI