RELIABILITY REPORT

FOR

**MAX1714AEEP**

PLASTIC ENCAPSULATED DEVICES

July 17,2006

# MAXIM INTEGRATED PRODUCTS

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## Conclusion

The MAX1714A successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents


**I. ........Device Description**
**II. ........Manufacturing Information**
**III. .......Packaging Information**
**V. ........Quality Assurance Information**
**VI. .......Reliability Evaluation**
**IV. .......Die Information**
**.....Attachments**


## I. Device Description

### A. General

The MAX1714 pulse-width modulation (PWM) controller provides the high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high-voltage batteries to generate low-voltage CPU core or chip-set/RAM supplies in notebook computers.

Maxim's proprietary Quick-PWM™ quick-response, constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The MAX1714 achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by an ability to drive very large synchronous-rectifier MOSFETs.

Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the +5V system supply instead of the battery) at a higher switching frequency allows the minimum possible physical size.

The MAX1714 is intended for CPU core, chipset, DRAM, or other low-voltage supplies as low as 1V. The MAX1714A is available in a 20-pin QSOP package and includes overvoltage protection. The MAX1714B is available in a 16-pin QSOP package with no overvoltage protection. For applications requiring VID compliance or DAC control of output voltage, refer to the MAX1710/MAX1711 data sheet. For a dual output version, refer to the MAX1715† data sheet.

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| V+ to AGND (Note 1) | -0.3V to +30V |
| VDD, VCC to AGND (Note 1) | -0.3V to +6V |
| PGND to AGND (Note 1) | ±0.3V |
| SHDN, PGOOD, OUT to AGND (Note 1) | -0.3V to +6V |
| ILIM, FB, REF, SKIP, | |
| TON to AGND (Notes 1, 2) | -0.3V to (VCC + 0.3V) |
| DL to PGND (Note 1) | -0.3V to (VDD + 0.3V) |
| BST to AGND (Note 1) | -0.3V to +36V |
| DH to LX | -0.3V to (BST + 0.3V) |
| LX to BST | -6V to +0.3V |
| REF Short Circuit to AGND | Continuous |
| Continuous Power Dissipation (TA = +70°C) | |
| 20-Pin QSOP (derate 9.1mW/°C above +70°C) | 727mW |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

**Note 1:** For the MAX1714B, AGND and PGND refer to a single pin designated GND.
**Note 2**: SKIP may be forced below -0.3V, temporarily exceeding the absolute maximum rating, disabling over/undervoltage fault detection for the purpose of debugging prototypes (Figure 6). Limit the current drawn to 5mA maximum.

## II. Manufacturing Information

A. Description/Function: High-Speed Step-Down Controller for Notebook Computers

B. Process: B12 (Standard 1.2 micron silicon gate CMOS)

C. Number of Device Transistors: 2721

D. Fabrication Location: California or Oregon, USA

E. Assembly Location: Malaysia, Philippines or Thailand

F. Date of Initial Production: September, 1999

## III. Packaging Information

A. Package Type: **20-pin QSOP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate or 100% Matte Tin

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-1101-0113

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1

## IV. Die Information

A. Dimensions: 105 x 79 mils

B. Passivation: $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: $SiO_2$

I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 397 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 2.77 \times 10^{-9}$

$\lambda$ = 2.77 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-5425) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B12/S12 Process results in a FIT rate of 0.10 @ 25°C and 1.78 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PX63 die type has been found to have all pins able to withstand a transient pulse of ±600V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

**Table 1**
Reliability Evaluation Test Results

**MAX1714AEEP**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 397 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | QSOP | 77 | 0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters<br>& functionality | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

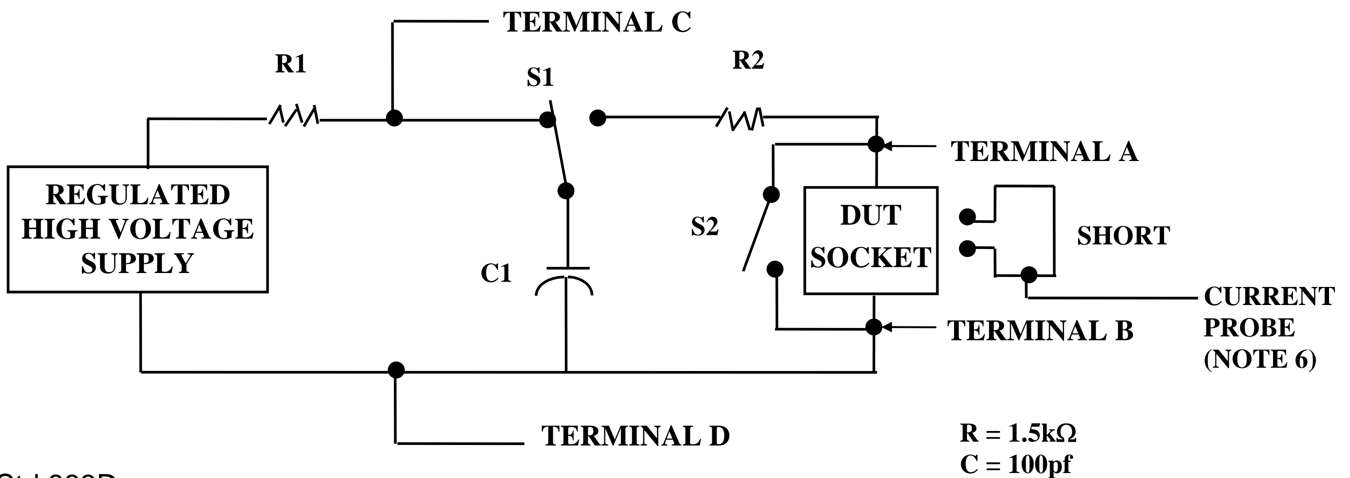
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

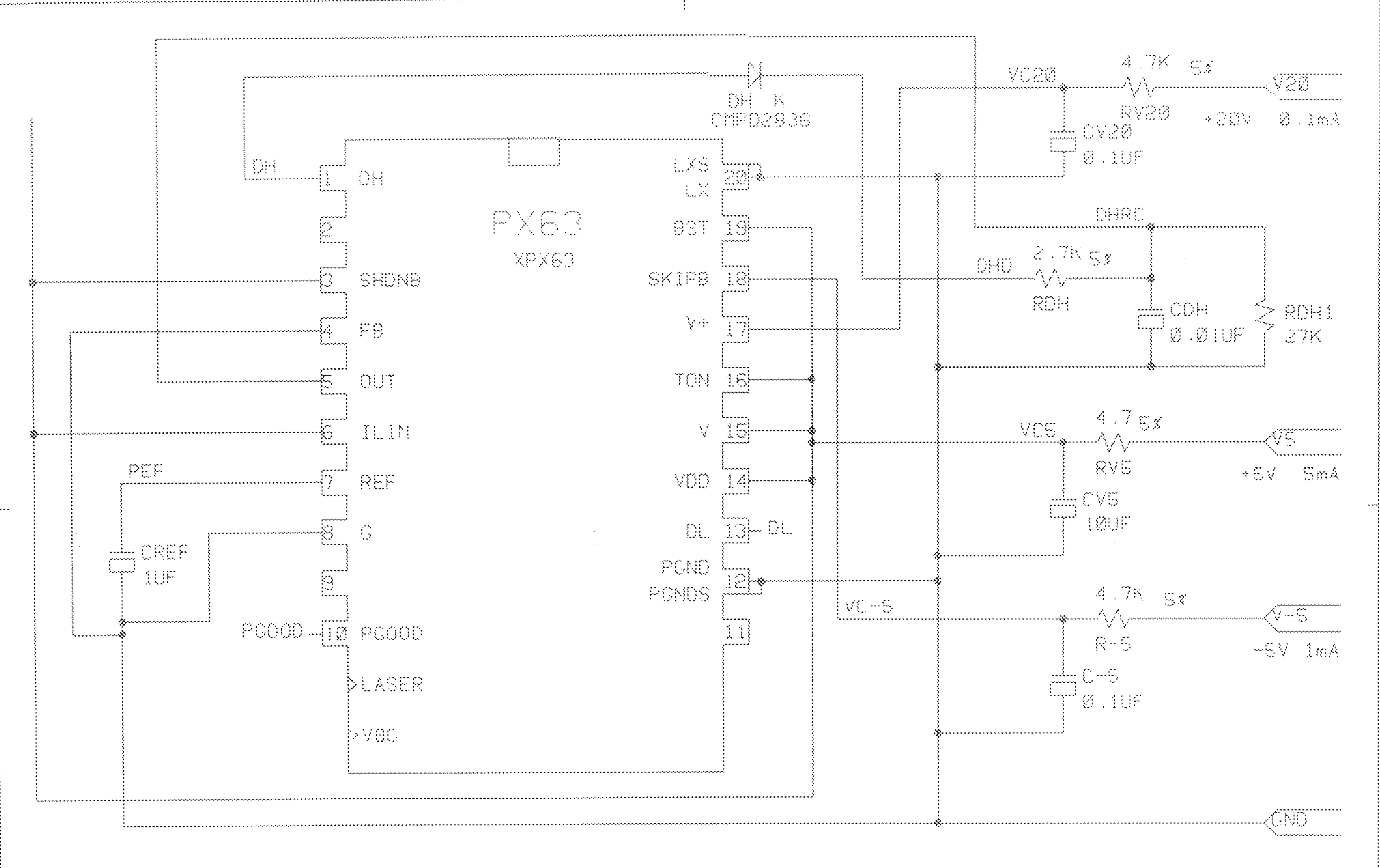
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



1
2
N/C
3
4
5
6
7
8
DIE I.D.
9
N/C
10
20
19
18
17
16
15
14
13
12
11
N/C

| PKG.CODE: E20-1 | | APPROVALS | DATE | | |
|---|---|---|---|---|---|
| CAV./PAD SIZE: 96X140 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1101-0113 | REV.: B |



DH
1 DH
2
3 SHDNB
4 FB
5 OUT
6 ILIN
7 REF
8 G
9
PGOOD 10 PGOOD
LASER
VBC
PX63
XPX63
LXS
LX 20
BST 19
SKIPB 18
V+ 17
TON 16
V 15
VDD 14
DL 13 DL
PGND
PGNDS 12
11
DH K
CMPD2836
PEF
CREF
1UF
VC20
4.7K 5%
RV20
V20
+20V 0.1mA
CV20
0.1UF
DHRC
DHD
2.7K 5%
RDH
CDH
0.01UF
RDH1
27K
VC5
4.7 5%
RV5
V5
+5V 5mA
CV5
10UF
VC-5
4.7K 5%
R-5
V-5
-5V 1mA
C-5
0.1UF
GND
MAXIM
CREATED: 12/31/97
BY: MG
LAST SAVED: 08:56:01 05-25-99
ENG2. -
SIZE
A
A
REVISION
00/00/00
DWG NO. -
BBOARD
PROJECT: PX51
DESC.: BURN-IN BOARD
FILE: BBOARD.DRW
SHEET 1 OF 1