RELIABILITY REPORT

FOR

MAX17112ETB+T

PLASTIC ENCAPSULATED DEVICES

June 12, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX17112ETB+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX17112 is a high-performance, step-up, DC-DC converter that provides a regulated supply voltage for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs). The MAX17112 incorporates current-mode, fixed-frequency (1MHz), pulse-width modulation (PWM) circuitry with a built-in, n-channel power MOSFET to achieve high efficiency and fast-transient response. The input overvoltage protection (OVP) function prevents damage to the MAX17112 from an input surge voltage (up to 24V). The high switching frequency (1MHz) allows the use of ultra-small inductors and low-ESR ceramic capacitors. The current-mode architecture provides fast-transient response to pulsed loads. A compensation pin (COMP) gives users flexibility in adjusting loop dynamics. The internal MOSFET can generate output voltages up to 20V from an input voltage between 2.6V and 5.5V. Soft-start slowly ramps the input current and is programmable with an external capacitor. The MAX17112 is available in a 10-pin TDFN package.

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II. Manufacturing Information

A. Description/Function:	High-Performance, Step-Up, DC-DC Converter
B. Process:	S45
C. Number of Device Transistors:	4624
D. Fabrication Location:	USA
E. Assembly Location:	China, Malaysia, Taiwan and Thailand
F. Date of Initial Production:	December 11, 2008

III. Packaging Information

A. Package Type:	10-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3476
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	9°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	9°C/W

IV. Die Information

A. Dimensions:	47 X 65 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.4 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 95 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.6 \times 10^{-9}$

λ = 11.6 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.04 @ 25°C and 0.69 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PF51 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114 (lot TSMZDQ002Q, D/C 0844)
ESD-MM: +/- 200V per JEDEC JESD22-A115 (lot TSMZDQ002Q, D/C 0844)
ESD-CDM: +/- 750V per JEDEC JESD22-C101 (lot TSMZDA084D, D/C 1117)

Latch-Up testing has shown that this device withstands a current of +/- 250mA (lot TSMZDQ002Q, D/C 0844).

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Table 1
Reliability Evaluation Test Results

MAX17112ETB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	95	0	TSMZDQ002D, D/C 0844

Note 1: Life Test Data may represent plastic DIP qualification lots.

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