RELIABILITY REPORT
FOR
MAX17075ETG+T
PLASTIC ENCAPSULATED DEVICES

April 29, 2012

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

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<th>Approved by</th>
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<tbody>
<tr>
<td>Richard Aburano</td>
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<tr>
<td>Quality Assurance</td>
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<tr>
<td>Manager, Reliability Engineering</td>
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</table>
Conclusion

The MAX17075ETG+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX17075 includes a high-voltage boost regulator, one high-current operational amplifier, two regulated charge pumps, and one MLG block for gate-driver supply modulation. The step-up DC-DC converter is a 1.2MHz current-mode boost regulator with a built-in power MOSFET. It provides fast load-transient response to pulsed loads while producing efficiencies over 85%. The built-in 160m (typ) power MOSFET allows output voltages as high as 18V boosted from inputs ranging from 2.5V to 5.5V. A built-in 7-bit digital soft-start function controls startup inrush currents. The gate-on and gate-off charge pumps provide regulated TFT gate-on and gate-off supplies. Both output voltages can be adjusted with external resistive voltage-dividers. The operational amplifier, typically used to drive the LCD backplane (VCOM), features high-output short-circuit current (±500mA), fast slew-rate (45V/μs), wide bandwidth (20MHz), and rail-to-rail outputs. The MAX17075 is available in a 24-pin thin QFN package with 0.5mm lead spacing. The package is a square (4mm x 4mm) with a maximum thickness of 0.8mm for ultra-thin LCD design. It operates over the -40°C to +85°C temperature range.
II. Manufacturing Information

A. Description/Function: Boost-Regulator with Integrated Charge Pumps, Switch Control, and High-Current Op Amp

B. Process: S45
C. Number of Device Transistors: 10458
D. Fabrication Location: USA
E. Assembly Location: China, Malaysia, Taiwan and Thailand
F. Date of Initial Production: August 19, 2008

III. Packaging Information

A. Package Type: 24-pin TQFN 4x4
B. Lead Frame: Copper
C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1.3 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-9000-3108
H. Flammability Rating: Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1
J. Single Layer Theta Ja: 48°C/W
K. Single Layer Theta Jc: 3°C/W
L. Multi Layer Theta Ja: 36°C/W
M. Multi Layer Theta Jc: 3°C/W

IV. Die Information

A. Dimensions: 79 X 79 mils
B. Passivation: Si3N4/SiO2 (Silicon nitride/ Silicon dioxide)
C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization: None
E. Minimum Metal Width: Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing: Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions: None
H. Isolation Dielectric: SiO2
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:  Richard Aburano (Manager, Reliability Engineering)  
                                Don Lipps (Manager, Reliability Engineering)  
                                Bryan Preeshl (Vice President of QA)  

B. Outgoing Inspection Level:  0.1% for all electrical parameters guaranteed by the Datasheet.  
                               0.1% For all Visual Defects.  

C. Observed Outgoing Defect Rate:  < 50 ppm  

D. Sampling Plan:  Mil-Std-105D  

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( \( \lambda \)) is calculated as follows:

\[
\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2} 
\]  

(Chi square value for MTTF upper limit)  

\( \lambda = 22.9 \times 10^{-9} \)  
\( \lambda = 22.9 \text{ F.I.T. (60% confidence level @ 25°C)} \)  

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.06 @ 25C and 1.0 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PF07 die type has been found to have all pins able to withstand a transient pulse of:  

ESD-HBM:  +/- 2500V per JEDEC JESD22-A114 (lot SLYZEQ002B, D/C 0836)  
ESD-MM:  +/- 250V per JEDEC JESD22-A115 (lot TLYZFA094A, D/C 1124)  

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78 (lot SLYZEQ002B, D/C 0836).
### Table 1
Reliability Evaluation Test Results

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test (Note 1)</td>
<td>Ta = 135C</td>
<td>DC Parameters &amp; functionality</td>
<td>48</td>
<td>0</td>
<td>SLYZEQ002B, D/C 0836</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Time = 192 hrs.</td>
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Note 1: Life Test Data may represent plastic DIP qualification lots.