Conclusion

The MAX1626 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX1626 step-down DC-DC switching controller provides high efficiency over loads ranging from 1mA to more than 2A. A unique current-limited, pulse-frequency-modulated (PFM) control scheme operates with up to a 100% duty cycle, resulting in very low dropout voltages. This control scheme eliminates minimum load requirements and reduces the supply current under light loads to 90μA (versus 2mA to 10mA for common pulse-width modulation controllers).

This step-down controller drives an external P-channel MOSFET, allowing design flexibility for applications to 12W or higher. Soft-start reduces current surges during start-up. A high switching frequency (up to 300kHz) and operation in continuous-conduction mode allows the use of tiny surface-mount inductors. Output capacitor requirements are also reduced, minimizing PC board area and system costs.

The output voltage is preset at 5V or 3.3V for the MAX1626. Input voltages can be up to 16.5V. The MAX1626 is a functional upgrade for the MAX1649.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, V+ to GND</td>
<td>-0.3V, +17V</td>
</tr>
<tr>
<td>OUT, FB, /3/5, SHDN, REF, CS, EXT to GND</td>
<td>-0.3V, (V+ + 0.3V)</td>
</tr>
<tr>
<td>Maximum Current at REF (I_REF)</td>
<td>15mA</td>
</tr>
<tr>
<td>Maximum Current at EXT (I_EXT)</td>
<td>50mA</td>
</tr>
<tr>
<td>Storage Temp.</td>
<td>-65°C to +160°C</td>
</tr>
<tr>
<td>Lead Temp. (10 sec.)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td></td>
</tr>
<tr>
<td>8-Pin SO</td>
<td>471mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td></td>
</tr>
<tr>
<td>8-Pin SO</td>
<td>5.88mW/°C</td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: 5V/3.3V, 100% Duty-Cycle, High-Efficiency, Step-Down DC-DC Controller
B. Process: SG5 (Standard 5 micron silicon gate CMOS)
C. Number of Device Transistors: 1627
D. Fabrication Location: Oregon, USA
E. Assembly Location: Philippines, Malaysia, or Korea
F. Date of Initial Production: May, 1996

III. Packaging Information

A. Package Type: 8 Lead Small Outline
B. Lead Frame: Copper
C. Lead Finish: Solder Plate
D. Die Attach: Silver-filled Epoxy
E. Bondwire: Gold (1.3 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: # 05-1701-0271
H. Flammability Rating: Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 81 x 105 mils
B. Passivation: Si$_3$N$_4$/SiO$_2$ (Silicon nitride/Silicon dioxide)
C. Interconnect: Aluminum/Si (Si = 1%)
D. Backside Metallization: None
E. Minimum Metal Width: 5 microns (as drawn)
F. Minimum Metal Spacing: 5 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO$_2$

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information
A. Quality Assurance Contacts:  
Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director)  
Kenneth Huening (Vice President)  

B. Outgoing Inspection Level:  
0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.  

C. Observed Outgoing Defect Rate:  
< 50 ppm  

D. Sampling Plan:  
Mil-Std-105D  

VI. Reliability Evaluation  

A. Accelerated Life Test  
The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:  

$$ \lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 480 \times 2} $$  
(Chi square value for MTTF upper limit)  

$$ \lambda = 2.26 \times 10^{-9} $$  

$$ \lambda = 2.26 \text{ F.I.T. (60% confidence level @ 25°C)} $$  

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-5166) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1M).  

B. Moisture Resistance Tests  
Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.  

C. E.S.D. and Latch-Up Testing  
The PW72 die type has been found to have all pins able to withstand a transient pulse of ±3000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±150mA.
Table 1
Reliability Evaluation Test Results

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong></td>
<td>Ta = 135°C</td>
<td>DC Parameters</td>
<td>480</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Moisture Testing</strong></td>
<td>Ta = 121°C</td>
<td>DC Parameters</td>
<td>SO</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>P = 15 psi.</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RH = 100%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 168hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>85/85</strong></td>
<td>Ta = 85°C</td>
<td>DC Parameters</td>
<td>77</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RH = 85%</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 1000hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong></td>
<td>-65°C/150°C</td>
<td>DC Parameters</td>
<td>77</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1000 Cycles</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Method 1010</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th>Terminal A</th>
<th>Terminal B</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Each pin individually connected to terminal A with the other floating)</td>
<td>(The common combination of all like-named pins connected to terminal B)</td>
</tr>
<tr>
<td>1. All pins except V_{PS1} 3/</td>
<td>All V_{PS1} pins</td>
</tr>
<tr>
<td>2. All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, +V_{S}, -V_{S}, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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Mil Std 883D
Method 3015.7
Notice 8
ONCE PER BOARD

ONCE PER DEVICE

PS1 \( I = \)
PS2 \( I = \)
PS3 \( I = \)
PS4 \( I = \)
PS5 \( I = \)
PS6 \( I = \)
\(+15V\)
\( I < 2mA \)

\( 2\Omega \)
\( .1\mu F \)

CLK0 \( \text{FREQ=} \)
CLK1 \( \text{FREQ=} \)
CLK2 \( \text{FREQ=} \)
CLK3 \( \text{FREQ=} \)
CLK4 \( \text{FREQ=} \)

GND

NOTES:
1. TEMPERATURE: 125°C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150°C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL [X] HR/883

SPEC. NO. 06-5166 REV: A
DATE: 11/24/95

MAXIM BURN-IN SCHEMATIC
DEVICE TYPE(S):
MAX1626/1627

DRAWN BY: