RELIABILITY REPORT FOR

MAX15096GWE+T / MAX15096AGWE+T

WAFER LEVEL DEVICES

November 6, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineer

Conclusion

The MAX15096GWE+T / MAX15096AGWE+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX15096/MAX15096A/MAX15096D ICs are integrated solutions for hot-swap applications requiring the safe insertion and removal of circuit line cards from a live backplane. They can also be used as electronics circuit breaker for hard drive and solid-state drive and fans. The devices integrate a hot-swap controller, 12m (typ) power MOSFET, and an electronic circuit-breaker protection in a single package. The devices are designed for protection of 2.7V to 18V supply voltages. These devices implement a foldback current limit during startup to control inrush current, lowering di/dt and keeping the MOSFET operating under safe operating area (SOA) conditions. After the startup cycle is complete, on-chip comparators provide VariableSpeed/BiLevel(tm) protection against short-circuit and overcurrent faults, and immunity against system noise and load transients. The load is disconnected in the event of a fault condition. The devices are factory calibrated to deliver accurate overcurrent protection with ±10% accuracy. During a fault condition, PG goes low and the devices latch off (MAX15096) or automatic retry (MAX15096A); the output could also be discharged after a fault event (MAX15096D). The devices feature an IN-to-OUT short-circuit detection before startup. The devices provide a power-MOSFET GATE pin to program the slew rate during startup by adding an external capacitor. The devices have an undervoltage/overvoltage input pin (UVOV) that can detect an undervoltage/overvoltage fault and disconnect the IN from the OUT. Additional features include internal overtemperature protection and a power-good output (PG). The devices are available in a 16-bump, 2mm x 2mm wafer-level package (WLP) and are rated over the -40°C to +105°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	2.7V to 18V, 6A Integrated Hot-Swap/Electronic Circuit Breaker
B. Process:	S18
C. Number of Device Transistors:	13012
D. Fabrication Location:	Japan
E. Assembly Location:	Japan
F. Date of Initial Production:	March 28, 2014

III. Packaging Information

A. Package Type:	16-bump WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-5575
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	49°C/W
M. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	80.3149 X 80.3149 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25°C and 6.96 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The NS11-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX15096GWE+T / MAX15096AGWE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.