RELIABILITY REPORT

FOR

MAX14528ETA+

PLASTIC ENCAPSULATED DEVICES

February 24, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX14528ETA+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX14527/MAX14528 overvoltage protection devices feature a low 100m (typ) RON internal FET and protect low-voltage systems against voltage faults up to +28V. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components. The overvoltage protection threshold can be adjusted with optional external resistors to any voltage between 4V and 8V. With the OVLO input set below the external OVLO select voltage, the MAX14527/MAX14528 automatically choose the internal ±2.5% accurate trip thresholds. The internal overvoltage thresholds (OVLO) are preset to 5.75V typical (MAX14527) or 6.76V typical (MAX14528). The MAX14527/MAX14528 are also protected against overcurrent events with an internal thermal shutdown. The MAX14527/MAX14528 are offered in a small, 8-pin TDFN-EP package and operate over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	Adjustable Overvoltage Protector with High Accuracy
B. Process:	S4
C. Number of Device Transistors:	2677
D. Fabrication Location:	Texas
E. Assembly Location:	UTL Thailand
F. Date of Initial Production:	October 25, 2008

III. Packaging Information

A. Package Type:	8-pin TDFN 2x2
B. Lead Frame:	
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Jc:	10.8°C/W
K. Multi Layer Theta Ja:	83.9°C/W
L. Multi Layer Theta Jc:	36.6°C/W

IV. Die Information

A. Dimensions:	35 X 64 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 47 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.8 \times 10^{-9}$

$\lambda = 22.8$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S45US Process results in a FIT Rate of 0.9 @ 25C and 13.84 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The AJ64-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

Table 1
Reliability Evaluation Test Results

MAX14528ETA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	47	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data