RELIABILITY REPORT

FOR

MAX13035EETE+

PLASTIC ENCAPSULATED DEVICES

October 10, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX13035EETE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX13030E-MAX13035E 6-channel, bidirectional level translators provide the level shifting necessary for 100Mbps data transfer in multivoltage systems. The MAX13030E-MAX13035E are ideally suited for memory-card level translation, as well as generic level translation in systems with six channels. Externally applied voltages, VCC and VL, set the logic levels on either side of the device. Logic signals present on the VL side of the device appear as a higher voltage logic signal on the VCC side of the device and vice versa. The MAX13035E features a CLK_RET output that returns the same clock signal applied to the CLK_VL input. The MAX13030E-MAX13035E operate at full speed with external drivers that source as little as 4mA output current. Each I/O channel is pulled up to VCC or VL by an internal 30Î¼A current source, allowing the MAX13030E-MAX13035E to be driven by either push-pull or open-drain drivers. The MAX13030E-MAX13034E feature an enable (EN) input that places the device into a low-power shutdown mode when driven low. The MAX13030E-MAX13035E features an automatic shutdown mode that disables the part when VCC is less than VL. The state of I/O VCC_ and I/O VL_ during shutdown is chosen by selecting the appropriate part version (see *Ordering Information/Selector Guide* located within the full datasheet). The MAX13030E-MAX13035E accept VCC voltages from +2.2V to +3.6V and VL voltages from +1.62V to +3.2V, making them ideal for data transfer between low-voltage ASIC/PLDs and higher voltage systems. The MAX13030E-MAX13035E are available in 16-bump UCSP (2mm x 2mm) and 16-pin TQFN (4mm x 4mm) packages, and operate over the extended -40°C to +85°C temperature range.

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II. Manufacturing Information

A. Description/Function:	6-Channel High-Speed Logic-Level Translators
B. Process:	S4
C. Number of Device Transistors:	
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	July 22, 2006

III. Packaging Information

A. Package Type:	16-pin TQFN 4x4
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2710
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	59.3°C/W
K. Single Layer Theta Jc:	5.7°C/W
L. Multi Layer Theta Ja:	40°C/W
M. Multi Layer Theta Jc:	5.7°C/W

IV. Die Information

A. Dimensions:	80X80 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.04 @ 25C and 0.69 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot SZ45BQ001B, D/C 0642)

The LT03-5 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX13035EETE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SZ40BQ001B, D/C 0642

Note 1: Life Test Data may represent plastic DIP qualification lots

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