RELIABILITY REPORT
FOR
MAX11871ETM+ / MAX11871EET+ / MAX11871EVM+
PLASTIC ENCAPSULATED DEVICES
MAX11871EWJ+
WAFER LEVEL PRODUCTS

July 3, 2013

MAXIM INTEGRATED
160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Quality Assurance
Manager, Reliability Engineering
Conclusion

The MAX11871EWJ+T / MAX11871ETM+ / MAX11871EET+ / MAX11871EVM+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

TINI® products deliver unparalleled integration to consumer applications. The portfolio includes complete system-on-chip (SoC) solutions and codecs that integrate multiple functions to achieve advantages in board space. A flagship member of the TINI family, the MAX11871 is a fully integrated touch-screen controller SoC for space-constrained applications such as smartphones, e-readers, and small tablet PCs. The device offers the industry's highest SNR analog front-end (AFE) for capacitive touch sensing, a MAXQ® CPU for full backend processing, and a custom DSP coprocessor. The integration of a super-narrowband AFE provides breakthrough immunity to AC charger and LCD noise without any external components. The SoC offers the industry's highest SNR, enabling chip-on-flex and chip-on-board designs. With the MAX11871, customers can eliminate air-gap and shield layers to design thinner products capable of supporting noisy chargers, passive-stylus touch, and gloved-hand touch. The MAX11871 is designed to interface with projected capacitive touch screens, detect multiple touches, and produce an image of measured capacitance values. The device supports up to 20 drive and 12 sense channels for a total of 240 nodes, at up to 120 frames per second (fps). The device can provide XY coordinate data as well as Z “pressure” metric for each touch point. The device operates standalone or in conjunction with Maxim's TacTouch™ family of haptic controllers. When paired with a TacTouch tactile-feedback controller, the MAX11871 provides a near-zero-latency touch and haptic solution. The MAX11871 uses three separate supply voltage inputs: \( V_{AVDD} = 2.7\,\text{V to 3.6\,V} \), \( V_{DVDD} = 1.7\,\text{V to 1.9\,V} \), \( V_{DVDDIO} = V_{DVDD} \) to 3.6V. The device is available in a 48-pin UTQFN (6mm x 6mm x 0.5mm) with exposed pad and a 49-bump WLP (3.7mm x 3.7mm x 0.64mm). All devices are specified over the extended temperature range \((-40°C to +85°C)\).
II. Manufacturing Information

A. Description/Function: TINI Touch-Screen Controller SoC for Mutual Projected Capacitive Touch
B. Process: 0.18um CMOS
C. Number of Device Transistors: 1,148,208
D. Fabrication Location: Taiwan
E. Assembly Location: Japan Taiwan Thailand
F. Date of Initial Production: March 25, 2011

III. Packaging Information

A. Package Type: 49-bump WLP 61-ball BGA 48-pin ultraTQFN
B. Lead Frame: N/A N/A Copper
C. Lead Finish: N/A N/A 100% matte Tin
D. Die Attach: None Non-conductive Conductive
E. Bondwire: N/A (N/A mil dia.) Au (0.8 mil dia.) Au (0.8 mil dia.)
F. Mold Material: None Epoxy with silica filler Epoxy with silica filler
G. Assembly Diagram: #05-9000-4544 #05-9000-4980 #05-9000-4580
H. Flammability Rating: Class UL94-V0 Class UL94-V0 Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C Level 1 Level 3 Level 1
J. Single Layer Theta Ja: °C/W °C/W 38°C/W
K. Single Layer Theta Jc: °C/W °C/W 1°C/W
L. Multi Layer Theta Ja: 35°C/W 40.4°C/W 27°C/W
M. Multi Layer Theta Jc: °C/W 5.1°C/W 1°C/W

IV. Die Information

A. Dimensions: 142.9134X142.9134 mils
B. Passivation: Si3N4/SiO2 (Silicon nitride/ Silicon dioxide)
C. Interconnect: Aluminum / 0.5% Copper
D. Backside Metallization: None
E. Minimum Metal Width: 0.23 microns (as drawn)
F. Minimum Metal Spacing: 0.23 microns (as drawn)
G. Bondpad Dimensions:
H. Isolation Dielectric: SiO2
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:
   Richard Aburano (Manager, Reliability Engineering)
   Don Lipps (Manager, Reliability Engineering)
   Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level:
   0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate:
   < 50 ppm

D. Sampling Plan:
   Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\chi = \frac{1}{1000 \times 516 \times 78 \times 2} = 1.83$$

(Chi square value for MTTF upper limit)

$$\lambda = 22.8 \times 10^{-9}$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.8 \text{ F.I.T. (60% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the Process results in a FIT Rate of 0.7 @ 25C and 12.3 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QAFH0A035A, D/C 1210)

The FP31 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 4000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78, except pin A0. Pin A0 passes when the voltage is limited to the pin A0 AMR of 4V during the stress.
### Table 1
Reliability Evaluation Test Results

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test</td>
<td>Ta = 100°C</td>
<td>DC Parameters</td>
<td>78</td>
<td>0</td>
<td>QV8ZEQ003E, D/C 1122</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td>&amp; functionality</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Time = 1000 hrs.</td>
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<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.