RELIABILITY REPORT
FOR
MAX1162xxxB
PLASTIC ENCAPSULATED DEVICES

April 1, 2004

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by  Reviewed by
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Quality Assurance  Quality Assurance
Manager, Reliability Operations  Managing Director
The MAX1162 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX1162 low-power, 16-bit analog-to-digital converter (ADC) features a successive-approximation ADC, automatic power-down, fast 1.1µs wakeup, and a high-speed SPI™/QSPI™/MICROWIRE™-compatible interface. The MAX1162 operates with a single +5V analog supply and features a separate digital supply, allowing direct interfacing with +2.7V to +5.25V digital logic.

At the maximum sampling rate of 200ksps, the MAX1162 consumes only 2.5mA. Power consumption is only 12.5mW (AV_{DD} = DV_{DD} = +5V) at a 200ksps (max) sampling rate. AutoShutdown™ reduces supply current to 130µA at 10ksps and to less than 10µA at reduced sampling rates.

Excellent dynamic performance and low power, combined with ease of use and small package size (10-pin µMAX and 10-pin DFN) make the MAX1162 ideal for battery-powered and data-acquisition applications or for other circuits with demanding power consumption and space requirements.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVDD to AGND</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>DVDD to DGND</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>DGND to AGND</td>
<td>-0.3V to +0.3V</td>
</tr>
<tr>
<td>AIN, REF to AGND</td>
<td>-0.3V to (AVDD + 0.3V)</td>
</tr>
<tr>
<td>SCLK, CS to DGND</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>DOUT to DGND</td>
<td>-0.3V to (DVDD + 0.3V)</td>
</tr>
<tr>
<td>Maximum Current Into Any Pin</td>
<td>50mA</td>
</tr>
<tr>
<td>Operating Temperature Ranges</td>
<td></td>
</tr>
<tr>
<td>MAX1162_CUB</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>MAX1162_EUB</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td></td>
</tr>
<tr>
<td>10-Pin µMAX</td>
<td>444mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td></td>
</tr>
<tr>
<td>10-Pin µMAX</td>
<td>5.6mW/°C</td>
</tr>
</tbody>
</table>
II. Manufacturing Information

A. Description/Function: 16-Bit, +5V, 200ksps ADC with 10µA Shutdown
B. Process: S6 (Standard 0.6 micron silicon gate CMOS)
C. Number of Device Transistors: 12,100
D. Fabrication Location: California, USA
E. Assembly Location: Malaysia, Philippines or Thailand
F. Date of Initial Production: July, 2002

III. Packaging Information

A. Package Type: 10-Pin uMAX 10-Pin DFN
B. Lead Frame: Copper Copper
C. Lead Finish: Solder Plate Solder Plate
D. Die Attach: Silver-Filled Epoxy Silver-Filled Epoxy
E. Bondwire: Gold (1 mil dia.) Gold (1 mil dia.)
F. Mold Material: Epoxy with silica filler Epoxy with silica filler
G. Assembly Diagram: #05-2101-0039 #05-9000-0405
H. Flammability Rating: Class UL94-V0 Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-A: Level 1 Level 1

IV. Die Information

A. Dimensions: 62 x 78 mils
B. Passivation: Si$_3$N$_4$/SiO$_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect: Aluminum/Si (Si = 1%)
D. Backside Metallization: None
E. Minimum Metal Width: 0.6 microns (as drawn)
F. Minimum Metal Spacing: 0.6 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO$_2$
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:
   Jim Pedicord (Manager, Reliability Operations)
   Bryan Preeshl (Managing Director)
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level:
   0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

   $\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 157 \times 2}$
   (Chi square value for MTTF upper limit)

   $\lambda = 6.92 \times 10^{-9}$

   $\lambda = 6.92 \text{ F.I.T. (60% confidence level @ 25°C)}$

   This low failure rate represents data collected from Maxim’s reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5715) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

   Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

   The AC23 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500 \text{V}$ per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250 \text{mA}$. 
Table 1
Reliability Evaluation Test Results

MAX1162xxxB

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test (Note 1)</td>
<td>Ta = 135°C Biased</td>
<td>DC Parameters &amp; functionality</td>
<td>SOT</td>
<td>157</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Moisture Testing (Note 2)</td>
<td>Pressure Pot</td>
<td>Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td>SOT</td>
<td>77</td>
</tr>
<tr>
<td></td>
<td>85/85</td>
<td>Ta = 85°C RH = 85% Biased Time = 1000hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
</tr>
<tr>
<td>Mechanical Stress (Note 2)</td>
<td>Temperature Cycle</td>
<td>-65°C/150°C 1000 Cycles Method 1010</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th></th>
<th>Terminal A (Each pin individually connected to terminal A with the other floating)</th>
<th>Terminal B (The common combination of all like-named pins connected to terminal B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

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Mil Std 883D
Method 3015.7
Notice 8
DEVICES: MAX 1062 AND 1162
PACKAGE: 10uMAX
MAX. EXPECTED CURRENT = 5mA