RELIABILITY REPORT
FOR MAX11068GUU+
PLASTIC ENCAPSULATED DEVICES

March 29, 2010

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Manager, Reliability Operations
Conclusion

The MAX11068GUU+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

The MAX11068 is a programmable, highly integrated, high-voltage, multicell battery sensor and digitizer. It is optimized for use with batteries used in automotive systems, hybrid electric battery packs, and electric cars. The highly integrated battery sensor incorporates a simple state machine and a high-speed communication bus.
II. Manufacturing Information

A. Description/Function: Multicell, High-Voltage, Automotive Battery Sensor and Digitizer
B. Process: S45J
C. Number of Device Transistors: 78489
D. Fabrication Location: California, Texas or Japan
E. Assembly Location: Malaysia
F. Date of Initial Production: July 24, 2009

III. Packaging Information

A. Package Type: 38-pin TSSOP
B. Lead Frame: Copper
C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-9000-3635
H. Flammability Rating: Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 3
J. Single Layer Theta Ja: 73°C/W
K. Single Layer Theta Jc: 11°C/W
L. Multi Layer Theta Ja: 63°C/W
M. Multi Layer Theta Jc: 11°C/W

IV. Die Information

A. Dimensions: 108 X 202 mils
B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization: None
E. Minimum Metal Width: Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing: Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO₂
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts:  
   Richard Aburano (Manager, Reliability Operations)  
   Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level:  
   0.1% for all electrical parameters guaranteed by the Datasheet.  
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate:  
   < 50 ppm

D. Sampling Plan:  
   Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

   \[
   \lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 45 \times 2} 
   \]

   (Chi square value for MTTF upper limit)

   \[
   (where \ 4340 = Temperature \ Acceleration \ factor \ assuming \ an \ activation \ energy \ of \ 0.8eV)
   \]

   \[\lambda = 24.4 \times 10^{-9}\]

   \[\lambda = 24.4 \text{ F.I.T. (60% confidence level @ 25°C)}\]

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL).

B. Moisture Resistance Tests

   The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

   The UC38 die type has been found to have all pins able to withstand a transient pulse of

   ESD-HBM: +/- 2500V per JEDEC JESD22-A114
   ESD-CDM: +/- 750V per JEDEC JESD22-C101
   ESD-MM: +/- 200V per JEDEC JESD22-A115

   Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78, except for one pin CP- under the condition that all "C" pins are treated as voltage pins. This is due to the fact that all "C" pins are always connected to power supplies through resistors. This configuration for the "C" pins is not likely to be at risk for latch-up per JEDEC JESD78 Annex A. Some voltage limitations were necessary because of the limitations of the commercial latch-up tester due to the unique cell-pin to cell-pin voltage restrictions in this part. Pin CP- passed the negative current injection stress to -25mA. In system applications, pin CP- must only be connected to companion pin CP+ and nothing else through a 0.01uF external capacitor. Such a configuration is recognized by JEDEC JESD78 Annex A as a very unlikely source for latch-up on CP- (and CP+).
Table 1
Reliability Evaluation Test Results

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Life Test</td>
<td>Ta = 135°C</td>
<td>DC Parameters &amp; functionality</td>
<td>45</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 192 hrs.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Moisture Testing</td>
<td>Ta = 130°C</td>
<td>DC Parameters &amp; functionality</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>RH = 85%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Biased</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time = 96hrs.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mechanical Stress</td>
<td>-65°C/150°C</td>
<td>DC Parameters &amp; functionality</td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1000 Cycles</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Method 1010</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data