RELIABILITY REPORT
FOR
DG409xxx
PLASTIC ENCAPSULATED DEVICES

August 21, 2003

MAXIM INTEGRATED PRODUCTS
120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by  Reviewed by
Jim Pedicord  Bryan J. Preeshl
Quality Assurance  Quality Assurance
Reliability Lab Manager  Executive Director
Conclusion

The DG409 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim’s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim’s quality and reliability standards.

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I. Device Description

A. General

Maxim’s redesigned DG409 CMOS analog multiplexer now feature guaranteed matching between channels (8 max) and flatness over the specified signal range (9 max). This low on-resistance mux (100 max) conducts equally well in either direction and features guaranteed low charge injection (15pC max). In addition, it offers low input off-leakage current over temperature—less than 5nA at +85°C.

The DG409 is a dual 4-channel multiplexer/demultiplexer, operating with a +5V to +30V single supply and with ±5V to ±20V dual supplies. ESD protection is guaranteed to be greater than 2000V per Method 3015.7 of MIL-STD-883. This improved mux is pin-compatible plug-in upgrade for the industry standard DG408.

B. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Referenced to V-</td>
<td></td>
</tr>
<tr>
<td>V+</td>
<td>-0.3V, 44V</td>
</tr>
<tr>
<td>GND</td>
<td>-0.3V, 25V</td>
</tr>
<tr>
<td>Digital Inputs, S, D (Note 1)</td>
<td>(V- - 2V) to (V+ + 2V) or30mA, (whichever occurs first)</td>
</tr>
<tr>
<td>Continuous Current (any terminal)</td>
<td>30mA</td>
</tr>
<tr>
<td>Peak Current, S, D (pulsed at 1ms, 10% duty cycle max)</td>
<td>100mA</td>
</tr>
<tr>
<td>Operating Temperature Ranges</td>
<td></td>
</tr>
<tr>
<td>DG409C</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>DG409D,E</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Voltage Referenced to V-</td>
<td></td>
</tr>
<tr>
<td>V+</td>
<td>44V</td>
</tr>
<tr>
<td>GND</td>
<td>25V</td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td></td>
</tr>
<tr>
<td>16-Pin DIP</td>
<td>842mW</td>
</tr>
<tr>
<td>16-Pin NSO</td>
<td>696mW</td>
</tr>
<tr>
<td>16-Pin TSSOP</td>
<td>755mW</td>
</tr>
<tr>
<td>Derates above +70°C</td>
<td></td>
</tr>
<tr>
<td>16-Pin DIP</td>
<td>10.53mW/°C</td>
</tr>
<tr>
<td>16-Pin SO</td>
<td>8.7mW/°C</td>
</tr>
<tr>
<td>16-Pin TSSOP</td>
<td>9.4mW/°C</td>
</tr>
</tbody>
</table>

Note 1: Signals on Sx, Dx, or INx exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.
II. Manufacturing Information

A. Description/Function: Improved, Dual 4-Channel, CMOS Analog Multiplexers
B. Process: S5HV (Medium voltage 5 micron silicon gate CMOS)
C. Number of Device Transistors: 122
D. Fabrication Location: Oregon, USA
E. Assembly Location: Philippines, Malaysia or Thailand
F. Date of Initial Production: January, 1994

III. Packaging Information

A. Package Type: 16-Lead NSO, 16-Lead TSSOP, 16-Lead PDIP
B. Lead Frame: Copper, Copper, Copper
C. Lead Finish: Solder Plate, Solder Plate, Solder Plate
D. Die Attach: Silver-filled Epoxy, Silver-filled Epoxy, Silver-filled Epoxy
E. Bondwire: Gold (1.3 mil dia.), Gold (1.0 mil dia.), Gold (1.3 mil dia.)
F. Mold Material: Epoxy with silica filler, Epoxy with silica filler, Epoxy with silica filler
G. Assembly Diagram: # 05-0301-0551, # 05-0301-0873, # 05-0301-0550
H. Flammability Rating: Class UL94-V0, Class UL94-V0, Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1, Level 1, Level 1

IV. Die Information

A. Dimensions: 80 x 136 mils
B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/Silicon dioxide)
C. Interconnect: Aluminum/Si (Si = 1%)
D. Backside Metallization: None
E. Minimum Metal Width: 5 microns (as drawn)
F. Minimum Metal Spacing: 5 microns (as drawn)
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO₂
I. Die Separation Method: Wafer Saw
V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
   Bryan Preeshl (Executive Director of QA)
   Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
   0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

   The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate \( \lambda \) is calculated as follows:

   \[
   \lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 480 \times 2} \quad \text{(Chi square value for MTTF upper limit)}
   \]

   Temperature Acceleration factor assuming an activation energy of 0.8eV

   \[
   \lambda = 2.26 \times 10^{-9} \quad \lambda = 2.26 \text{ F.I.T.} \quad (60\% \text{ confidence level @ } 25\degree C)
   \]

   This low failure rate represents data collected from Maxim’s reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5584) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

   Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

   The AG56-1 die type has been found to have all pins able to withstand a transient pulse of ±3000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.
**Table 1**  
Reliability Evaluation Test Results

DG409xxx

<table>
<thead>
<tr>
<th>TEST ITEM</th>
<th>TEST CONDITION</th>
<th>FAILURE IDENTIFICATION</th>
<th>PACKAGE</th>
<th>SAMPLE SIZE</th>
<th>NUMBER OF FAILURES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static Life Test</strong> (Note 1)</td>
<td>Ta = 135°C Biased Time = 192 hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>480</td>
<td>0</td>
</tr>
<tr>
<td><strong>Moisture Testing</strong> (Note 2)</td>
<td>Pressure Pot Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td>PDIP NSO TSSOP</td>
<td>77 77 77</td>
<td>0 0 0</td>
</tr>
<tr>
<td></td>
<td>85/85 Ta = 85°C RH = 85% Biased Time = 1000hrs.</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
<tr>
<td><strong>Mechanical Stress</strong> (Note 2)</td>
<td>Temperature Cycle Method</td>
<td>DC Parameters &amp; functionality</td>
<td></td>
<td>77</td>
<td>0</td>
</tr>
</tbody>
</table>

Note 1: Life Test Data may represent plastic DIP qualification lots.  
Note 2: Generic Package/Process data
TABLE II. Pin combination to be tested. 1/ 2/

<table>
<thead>
<tr>
<th></th>
<th>Terminal A (Each pin individually connected to terminal A with the other floating)</th>
<th>Terminal B (The common combination of all like-named pins connected to terminal B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>All pins except $V_{PS1}$ 3/</td>
<td>All $V_{PS1}$ pins</td>
</tr>
<tr>
<td>2.</td>
<td>All input and output pins</td>
<td>All other input-output pins</td>
</tr>
</tbody>
</table>

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

Mil Std 883D
Method 3015.7
Notice 8
PACKAGE: 16-NSO
Max current = (+10v)=10uA
MAX4590/4709 (+/- 15V) = 350uA. Rest of parts (+/-15v) = 50uA.