DELAY TIME AND RESET TIMEOUT PERIOD SET TO 1.1mS
Maxim Regulator Inhibit Jumper
TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.
MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR
CONNECT AGND TO GND AT OUTPUT CAPACITORS
SYNCHRONIZED TO OTHER LOWER CURRENT RAILS OPERATING AT 600 kHZ.

VCCINT RAIL SWITCHING FREQUENCY IS 400kHz AND SHOULD NOT BE

R226 1/10W 2.21K
R156 1/10W 2.2K
R514 1/10W 1400
R81 1/10W 1.7K Q23
C736 10V 10UF X7R
LXSNS 2 PLACES

REMOTE SENSE CONNECTIONS AT DUT PADS

DEFAULT = 0.95VDC

VCCINT 40A Regulator

CONNECT AGND TO GND AT OUTPUT CAPACITORS

MINIMUM 1 LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR
TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCITOR
CONNECT ACROSS FINS OF OUTPUT INDUCITOR

VCCINT 40A Regulator

TITLE: VCCINT 40A Regulator
DATE: 11/13/2014:10:59
DRAWN BY: RF

SHEET SIZE: B
REVISION: 01

SCHEM, ROHS COMPLIANT
TEST P/N: TSS0165
SCH P/N: 0381556
PCB P/N: 1280723
ASSY P/N: 0431811

MMSZ4680T1G
2.2V
D16
A

B

C

D

REMOTE SENSE CONNECTIONS AT DUT PADS

DEFAULT = 1.80VDC

VADJ 1V8 10A Regulator

TITLE: VADJ 1V8 10A Regulator

SCH P/N: 0381556

PCB P/N: 1280723

ASSY P/N: 0431811

DATE: 11/13/2014 10:59

REV. 01

DRAWN BY: RF

SHEET: 56 OF 66

PLAC LENGTH COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR.

CONNECT ACROSS PINS OF OUTPUT INDUCTOR ANDAVJRFAULT CONNECTIONS TO AVOID CONTRIBUTIONS TO CURRENT MEASUREMENTS.

MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR CONNECT ACROSS PINS OF OUTPUT INDUCTOR.

PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR.
**VCC1V2 3A Regulator**

**INTUNE DIGITAL POL REGULATOR**

**MAX15303**

**REMOTE SENSE CONNECTIONS AT DUT PADS**

**DEFAULT = 1.20VDC**

**Connect across pins of output inductor.**

**Minimum load required.** Must be connected before sense resistor to avoid contribution to current measurements.

**PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR.**
**NOTES**

1. Capacitors should be placed as close as possible to Pin12 and 14.
NOTES

1. Capacitors should be placed as close as possible to Pin2 and 14
DEFAULT = 1.80VDC

MGTVCCAUX 1A Regulator

R952  Pin 1 of 10.2K resistor must be routed as a sense line directly to a U1 power pin

PLACE NEAR U1 FPGA
TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

CONNECT ACROSS PINS OF OUTPUT INDUCTOR

REMOTE SENSE CONNECTIONS AT DUT PADS

DEFAULT = 3.30VDC

PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

MINIMUM IN LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.