

# 73M1866B/73M1966B GUI User Guide

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# 1 Introduction

The 73M1866B/73M1966B Graphical User Interface (GUI) provides control of the 73M1866B and 73M1966B registers. The GUI is used to configure the 73M1866B and 73M1966B demo boards and to read the status conditions of these boards. This document applies to GUI software version 1.3.

The GUI can be use with either the Demo Board or the Keychain Board. The GUI cannot be used if the SPI is connected to a host device. For example, if a Keychain Board is embedded in an application, use the appropriate driver (MIPS, ARM, etc.) to configure the Keychain Board.

Install the GUI on a PC running Microsoft Windows<sup>®</sup> versions XP, Me or 2000. The installation requires one megabyte of disk storage.

In this user guide, the 73M1866B and 73M1966B will be collectively referred to as the 73M1x66B.

The FPGA controls are not for customer use. Do not change the parameters on the FPGA tab.

Similarly, do not select FPGA Functions from the Controls menu or use the functions on the FPGA Memory Functions screen.

# 2 Getting Started

This section describes how to install, start and use the GUI software.

#### 2.1 GUI Installation

Load the GUI software from the CD onto the PC that will be used to control the configuration of the 73M1x66B Demo Board.

Run       ? \leq         Type the name of a program, folder, document, or Internet resource, and Windows will open it for you.	If the GUI software does not run automatically when the CD is installed, select Start $\rightarrow$ Run and browse the CD drive for Teridian_73M1966_1_3_SETUP.EXE.
Open: Documents\Teridian_73M1966B_1_3_SETUP.EXE"	Select OK. The following window appears.
Open File - Security Warning         The publisher could not be verified. Are you sure you want to run this software?         Image: Software         Image: Software to run?	Select Run.
InstallShield Self-extracting EXE This will install 73M1966B. Do you wish to continue?	Select Yes to continue.
Yes No	The following window appears.
Readme Information         Information:         Ver 1.3 11/29/2007         1. Additional changes made according to the "1966 GUI CF         Ver 1.2 10/19/2007         2. Add button to stop Continuous Poling.         3. Added "Go Off-Hock" & "Calibration" b         4. Bug "Cart Load Script after Reset with File" fixed.         5. Bug "Reset File pointer point to last choren file in PFGA1         6. Bug "Reset File pointer point to last choren file in PFGA1         7. "Memory Access Mode" remarked to "Internal Memory St.         8. Step Mode removed.         9. Read access to Gain registers R08 & R09 is blocked.         10. Register Bit Name changes.         Ver 1.1 06/14/2007         Ver 1.1 06/14/2007	This window lists the revisions of the GUI software and the improvements made in each revision.
KBack Next> Cancel	Select Next. The following window appears.



#### 2.2 Using the GUI

The 73M1866B or 73M1966B Demo Board must be set up before using the GUI. See the 73M1866B/73M1966B Demo Board User Manual for setup procedures.

To start the GUI using Windows XP, select Start  $\rightarrow$  All Programs  $\rightarrow$  Teridian  $\rightarrow$  Teridian 73M1966B.

The Register Access screen appears (see Figure 1). The screen is divided into a top half and a bottom half. The first row of the top half consists of five tabs: R00-R09, R0A-R12, R13-R1B, R1C-R25 and FPGA.

The R00-R09 tab displays the register map for the first ten 73M1966B registers. The contents of each named bit can be changed by checking or un-checking the box next to it. A checked box means that the bit is set to 1 and an un-checked box means that the bit is set to 0. As boxes are checked and unchecked, the values in the bottom half reflect the changes and turn red. Select new values by checking and un-checking register bits. Click the Write Red button to set the values. Notice that after writing the values, all previously red values turn black. Polling can be done by double clicking on the lower register map for the register you are interested in or using the "Read All" radio button.

🗟 Regist	Register Access								
R00-R09 FDA-R12 R13-R18 R1C-R25 FPGA									
R00	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
R01									
R02 R03							E cont		
R04	DIR7	DIR6	DIR5	I POLKDI	REVHSD3	REVHSD2	REVHSD1		
R05 R06	ENGPIO7	ENGPIO6		ENPCLKDT	ENAPOL	ENDET	🔽 ENSYNL	ENRGDT	
R07	POL/	I POL6	POL5				T DTST1	T DTSTO	
R08	TX-12dB	TX-6dB	TX+3.5dB	TX+2dB	TX+1dB	TX+0.5dB	TX+0.25dB	TX+.125dB	
	TE RX-12dB	I RX-6dB	T RX+3.5dB	T RX+2dB	T RX+1dB	T RX+U.5dB	T RX+0.25dB	T RX+.125dB	
Regist	ers (Double Clic	k on Register Add	tress to Read Sir	ngle Register) —			Bits in Orange	are Read-Only	
1966	B:						F BRCT		
	02	03 04 05	06 07 0	08 09		OD OE OF	<ul> <li>8-Bit</li> </ul>	© 16-Bit	
	10	E0 E4 B	00 00 0	00 00		90 80 80	1906 CID	(Hex): 0	
_10	12	13 14 15	16 17	18 <u>19</u> 1A	18 1C	1D 1E 1F	FPGA CID	(Hex): 1	
00	E5	80 22 08	D0 00 0	01 00 00	78 26	C5 00 E5	Poll Index (bex	1: 4	
_20	21 22	23 24	00_01	02 03	Write Red	Decid All	Value (bex		
9F	1F 3F	80 00	BF  00	00 00 -	Write All		Match: 6	Poll	
Reset	Options				Macro Fu	nctions			
C Re:	set to Default V	alues	Reset		Go Off-ł	look Calibrat	tion Ring	Voltage	
Re:	set to Script File ogram Files\Teri	8 dian\73W1966B\0	)ff-Hook (	C CTR-21	Go On-H	look SPI Res	set	-1.500V	
-Log Fi	le Settings	alar v om 1700D (c			1			Monitor 15.47 V	
Lo	g All Register Ac	cesses to File	📕 Log Status		TEP	AIDIS	N 1	58.75 mA	
					SEMICO		OBB	Stop	
					SEIVIGO	NDOCION C			

Figure 1: Register Access Screen – R00-R09 Tab

The bottom half of the Register Access screen shows the status of the entire 73M1x66B register set (in hex) and provides information and parameter controls.

Table 1 describes these controls.

Write Red Write All	Click Write Red to write all red values in the bottom half of the screen. Values become red when changed by checking or un-checking boxes in the top half of the screen. Click Write all to write all values (both read and black). After writing values, all values become black and remain black until another box is checked.
Read All	Click to read all current values from the board.
Settings BRCT BRCT S-Bit 16-Bit 1906 CID (Hex): 0 FPGA CID (Hex): 1	Select BRCT (BroadCasT) to send the same control data to all the 73M1966Bs in a daisy chain, ignoring their individual addresses. When using the 73M1966B in daisy chain mode, it is necessary to set the address of the 73M1966B that is being accessed. Each board has a 73M1906B and FPGA address. For example, the next downstream daisy chained 73M1966B board will have an address for its 73M1906B of 03h and its FPGA address will be 04h, and so on. See Section 5 of the 73M1866/73M1966 Data Sheet for a description of the control byte and the BRCT bit. The radio buttons allow the selection of 8-bit or 16-bit SPI operations.
Poll Index (hex): 1 Value (hex): FF Match: Poll	Implements the POLL function as described in Section 6.1 of the 73M1866B/73M1966B Data Sheet. The Index field corresponds to the INDX field (Register 0x19[3:0]). The Value field corresponds to the POLVAL field (Register 0x1F[7:0]). Index is the offset address of the register to be manually polled with the results placed in POLVAL. The Index value ranges from 0 to 6 only. Index 0 refers to Register 0x12, Index 1 to Register 0x13, etc. The Value field returns the content of the register corresponding to the specified Index. Enter the index in the Index box. Select Poll. When this register is polled, the value is read back in the Value box. After selecting Poll, a red dot next to Match means that the register was not properly written. A green dot proves that the register was properly written.
Reset Options     Reset to Default Values     Reset to Script File	Sets the registers to a default operating configuration. This is not the same as the default register settings after the 73M1x66 goes through a device reset. The default register settings may not be appropriate for all PCM test sets, so you may define your own default operating conditions.

Table 1: GUI Controls

Reset Options       Reset         Reset to Default Values       Reset         Reset to Script File       Reset         ridian\73M1966B\Off-Hook Operating Mode.tsf	Sets the registers to a user-defined configuration contained in a specified script file. This is used to quickly put the registers into a configuration and the 73M1x66 into operational mode without having to individually set the register bits. If you have a configuration that you will use again later, the configuration can be saved as a script. See Log All Register Accesses to File.
Log File Settings Log All Register Accesses to File Log Status C:\Program Files\Teridian\73M1966B\Initial Setup.log	Used to keep a record of all register accesses performed by the user. Once turned on, user transactions are recorded in the file specified in the window. This is used to record a sequence of operations that can be edited and saved as a script. To use the recorded configuration, see Reset to Script File.
Log File Set&ings ✓ Log All Register Accesses to File ✓ Log Status C:\Program Files\Teridian\73M1966B\Initial Setup.log	If Log Status is checked, all SPI transactions are recorded in the specified file, including those generated by the background line condition monitoring routine (line voltage, current, etc.). If Log Status is checked and line condition monitoring is activated, be aware that the log file is continuously increasing in size.
C U.S. C CTR-21 C Australian	The settings for the three most common termination impedances. These are U.S. ( $600 \Omega$ ), CTR-21 (complex) and Australian (Australian complex). Select one to set the termination impedance. After activating the Read All radio button, the currently valid impedance is indicated only if it is one of the three choices. If the currently valid impedance is not one of the three choices, none of the options will be shown as active.
Go Off-Hook	Goes Off-Hook.
Go On-Hook	Goes On-Hook.
Calibration	Calibrates the receive channel of the chipset.
SPI Reset	If the SPI transactions are corrupted for some reason, pressing this button resets the 73M1966B SPI state machine and restores proper communication between the 73M1966B and the GUI.
-1.500V	Updated with the most recent ring signal voltage as measured in R1A. This measurement is only valid during the on-hook state.
15.47 V 158.75 mA	CO or line emulator. The current reading is valid in off-hook mode only.
Stop	Stops the continuous line condition monitoring routine. Line voltage, current, etc. will not be written to the log file.
Start	Starts the continuous line condition monitoring routine. Line voltage, current, etc. will be written to the log file.

#### 2.2.1 Controls for Registers R00 to R09

The GUI represents 73M1x66B registers in the form Rhh, where hh is the hexadecimal address. The 73M1866B/73M1966B Data Sheet represents these same registers in the form 0xhh.

For detailed descriptions of 73M1x66B registers, see the 73M1866B/73M1966B Data Sheet. The tables below list the section numbers in the 73M1866B/73M1966B Data Sheet where additional information can be found about each bit.

R00-R09	ROA-R12 R	13-R1B   R1C-R2	5 FPGA					
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R00								1996
R01								
R02	TMEN					ENLPW		
R03	GPI07	GPIO6	GPIO5	PCLKDT	RGMON	DET	SYNL	RGDT
R04	DIR7	DIR6	DIR5		F REVHSD3	REVHSD2	REVHSD1	F REVHSDO
R05	ENGPIO7	ENGPIO6	ENGPIO5	ENPCLKDT	ENAPOL	ENDET	ENSYNL	ENRGDT
R06	F POL7	POL6	F POL5					
R07							DTST1	T DTSTO
R08	TX-12dB	TX-6dB	TX+3.5dB	TX+2dB	TX+1dB	TX+0.5dB	TX+0.25dB	TX+.125dB
R09	RX-12dB	🕅 RX-6dB	RX+3.5dB	□ RX+2dB	RX+1dB	RX+0.5dB	F RX+0.25dB	RX+.125dB

Register	Bit Name	Summary Description	Data Sheet Section
R02[7]	TMEN	Test Mode Enable	12.7
R02[2]	ENLPW	Enable Line Power	9.5
R03[7:5]	GPIOn	GPIO Pin Enable	7.5
R03[4]	PCLKDT	PCLK Error Detected	8.8
R03[3]	RGMON	Ringing Monitor $-0$ = silent, 1 = ringing	11.12
R03[2]	DET	Voltage Detection $-1$ = detection of one of three conditions	11.12
R03[1]	SYNL	Barrier Synchronization Loss has occurred	9.5
R03[0]	RGDT	Ring or Line Reversal Detection $-1 = a$ Latched Ring or Line Reversal Detection event	11.12
R04[7:5]	DIRn	GPIO Input/Output Select $-0 =$ GPIO pin is an output, 1 = GPIO pin an input	7.5
R04[3:0]	REVHSDn	Host-Side Device Revision	7.1
R05[7:5]	ENGPIOn	GPIO Enable	7.5
R05[4]	ENPCLKDT	Enable PCLK Detection	8.8
R05[3]	ENAPOL	Enable Automatic Polling	9.5
R05[2]	ENDET	Enable Voltage Detection	11.12
R05[1]	ENSYNL	Enable Synch Loss Detection	9.5
R05[0]	ENRGDT	Enable Ring Detection Interrupt	11.12
R06[7:5]	POLn	GPIO Interrupt Edge Selection	7.5
R07[1:0]	DTSTn	Digital Test Mode Select	12.7
R08	TXDGn	Transmitter Digital	8.8
R09	RXDGn	Receiver Digital Gain	8.8

## 2.2.2 Controls for Registers R0A to R12

R00-R09	ROA-R12 R1	13-R1B   R1C-R2	5 FPGA					
ROA	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ROB								
RUC		-						
ROE	IV LOKDET ▼ ERCVCO	ISLHS					E RGTH1	E RGTH0
ROF	ENFEH	PWDN	SLEEP				) Kann	i dine
R10				CMVSEL	CMTXG1	СМТХСО	CMRXG1	CMRXG0
R11	1000	1000	1000	1000	1000	10.00	10000	
R12	✓ OFH	ENDC	ENAC	ENSHL	ENLVD	ENFEL	ENDT	ENNOM

Register	Bit Name	Summary Description	Data Sheet Section
R0D[7]	LOKDET	Phase Locked Loop Lock Detect	7.4
R0D[6]	SLHS	Synchronized Lost Host Side	9.5
R0E[7]	FRCVCO	Force VCO	7.4
R0E[1:0]	RGTHn	Ring Detect Threshold	11.12
R0F[7]	ENFEH	Enable Front End Host	7.3
R0F[6]	PWDN	Power Down Mode	7.3
R0F[5]	SLEEP	Sleep Mode	7.3
R10[4]	CMVSEL	Call Progress Monitor Voltage Reference Select	7.6
R10[3:2]	CMTXGn	Transmit Path Gain Setting	7.6
R10[1:0]	CMRXGn	Receive Path Gain Setting	7.6
R12[7]	OFH	Off-Hook Enable	10.6
R12[6]	ENDC	Enable DC Transconductance Circuit	10.6
R12[5]	ENAC	Enable AC Transconductance Circuit	10.6
R12[4]	ENSHL	Enable Shunt Loading	10.6
R12[3]	ENLVD	LeV Detection (OVDET, UVDET, OIDET monitors)	10.6
R12[2]	ENFEL	Enable Front End Line-Side Circuit	10.6
R12[1]	ENDT	Enable Detectors	11.12
R12[0]	ENNOM	Enable Nominal Operation	10.6

## 2.2.3 Controls for Registers R13 to R1C

R00-R09	ROA-R12	13-R1B R1C-R2	5 FPGA					
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
R13	CIV1	C DCIVO	T ILM	ACCEN	F PLDM	C OVDTH	IDISPD	SEL16K
R14	TXBST	DAA1	DAA0		🕅 RXBST	T RLPNH	RXG1	T RXG0
R15	ENOLD	DISNTR	CHPSEN	CIDM	THEN	ENUVD	ENOVD	ENOID
R16	TXEN	RXEN	RLPNEN	ATEN	ACZ3	ACZ2	ACZ1	C ACZO
R17			RXOCEN					
R18	🗔 тята	TST2	TST1	🗆 туто				
R19	F POLL	MATCH		T IDL2	T INDX3	T INDX2	INDX1	T INDX0
R1A	RNG7	RNG6	RNG5	RNG4	RNG3	RNG2	RNG1	RNG0
R1B	LV7	✓ LV6	I LV5	I LV4	🔽 LV3	LV2	LV1	

Register	Bit Name	Summary Description	Data Sheet Section
R13[7:6]	DCIVn	DC Current Voltage Characteristic Control	10.6
R13[5]	ILM	Current Limit Enable – 0 = no limit, 1 = 42 mA current limit	10.6
R13[4]	ACCEN	AC Cancellation Enable	10.6
R13[3]	PLDM	Pulse Dialing Enable	10.6
R13[2]	OVDTH	Over-Voltage Threshold	11.12
R13[1]	IDISPD	Discharge and Pulse Dialing	10.6
R13[0]	SEL16K	Sample Rate Mode Configuration Select	8.8
R14[7]	TXBST	Transmit Boost	8.8
R14[6:5]	DAAn	Data Access Arrangement Used with TXBST to manage transmit level.	8.8
R14[3]	RXBST	Received Boost If set to 1, receive signal is increased by 20 dB.	8.8
R14[2]	RLPNH	Receive Low Pass Notch 0 = Selects Receive Low Pass Notch (RLPN) at 12 kHz. 1 = Selects RLPN at 16 kHz.	10.6
R14[1:0]	RXGn	Receive Gain Control	8.8
R15[7]	ENOLD	Enable Over-Load Detector	11.12
R15[6]	DISNTR	Disable No-Transition Timer	11.12
R15[5]	CHPSEN	Enable Chopper Stabilization	10.6
R15[4]	CIDM	Caller ID Mode	11.12
R15[3]	THEN	Enable Transhybrid Circuit	10.6
R15[2]	ENUVD	Enable Under Voltage Detector	11.12
R15[1]	ENOVD	Enable Over-Voltage Detector	11.12
R15[0]	ENOID	Enable Over-Current Detector	11.12
R16[7]	TXEN	Transmit Path Enable	8.8
R16[6]	RXEN	Receive Path Enable	8.8
R16[5]	RLPNEN	Receive Low Pass Notch Enable	10.6
R16[4]	ATEN	Active Termination Loop Enable	10.6
R16[3:0]	ACZn	Active Termination Loops	10.6
R17[5]	RXOCEN	Rx DC Offset Calibrate Enable	8.8
R18[7:4]	TESTn	Enable Loopback Mode	12.7
R19[7]	POLL	Polling Enable	6.1

Register	Bit Name	Summary Description	Data Sheet Section
R19[6]	MATCH	Polling Match	6.1
R19[4]	IDL2	Ring Detect Functions	7.3
R19[3:0]	INDXn	Index Address of the register to be manually polled with the results placed in POLVAL.	6.1
R1A[7:0]	RNGn	Result of Auxiliary A/D measuring the attenuated ring voltage.	11.12
R1B[7:1]	LVn	Line Voltage Reading	11.12

#### 2.2.4 Controls for Registers R1D to R23

R00-R09	ROA-R1	2   R13-F	(1B R1C-R2	5	FPGA										
	[7]		[6]		[5]		[4]		[3]		[2]		[1]		[0]
R1C	LC6		LC5	V	LC4	Г	LC3	Г	LC2	V	LC1	~	LC0		1000
R1D	REVL	SD3 🗖	REVLSD2	Г	REVLSD1	Γ	REVLSDO								
R1E	T ILMC	N L	UVDET	Г	OVDET	Γ	OIDET	Г	OLDT	Г	SLLS				
R1F	POLL	VAL7	POLLVAL6	V	POLLVAL5	Γ	POLLVAL4	Γ	POLLVAL3	~	POLLVAL2	Г	POLLVAL1	1	POLLVALO
R20	TPOL	. Г	TTS6	Г	TTS5	V	TTS4	~	TTS3	~	TTS2	~	TTS1	~	TTSO
R21	F RPOL	Г	RTS6	Г	RTS5	V	RTS4	~	RTS3	V	RTS2	~	RTS1	~	RTSO
R22	□ SR	Г	ADJ	V	RCS2	V	RCS1	~	RCS0	V	TCS2	~	TCS1	~	TCS0
R23	PCME	EN E	MASTER	Г	PCODE3	Г	PCODE2	Г	PCODE1	Г	PCODE0	Г	LIN		LAW
R24														Г	LB
R25															

Registers		Description	Data Sheet
			Section
R1C[7:1]	LCn	Loop Current	11.12
R1D[7:4]	REVLSDn	Line-Side Device Revision	7.1
R1E[7]	ILMON	Current Limit Mode On	10.6
R1E[6]	UVDET	Under-Voltage Detector	11.12
R1E[5]	OVDET	Over-Voltage Detector	11.12
R1E[4]	OIDET	Over-Current (I) Detector	11.12
R1E[3]	OLDET	Over-Load Detector	11.12
R1E[2]	SLLS	Synchronization Loss Line Side	9.5
R1F[7:0]	POLLVALn	Polling Value	6.1
		When polled, the content of the Line-Side Device Register	
R20[7]	TPOL	Transmit Polarity	8.8
R20[6:0]	TTSn	Transmit Time Slot	8.8
R21[7]	RPOL	Receive Polarity	8.8
R21[6:0]	RTSn	Receive Time Slot	8.8
R22[7]	SR	Sampling Rate Mode	8.8
R22[6]	ADJ	Adjacent Time Slots	8.8
R22[5:3]	RCSn	Receive Clock Slot	8.8
R22[2:0]	TCSn	Transmit Clock Slot	8.8
R23[7]	PCMEN	PCM Transmit Enable	8.8
R23[6]	MASTER	Master/Slave Mode	8.8
		0 = enables Slave Mode; 1 = enables Master Mode.	
R23[5:2]	PCODEn	PCM Clock Code	8.8
R23[1]	LIN	Linear Mode Enable	8.8
R23[0]	LAW	Law Compression Mode	8.8
		$0 =$ selects A-law; $1 =$ selects $\mu$ -law.	
R24[0]	LB	Enables PCM Loopback within the Host-Side Device.	12.7

# 3 Scripts

If you have a configuration that will be used again later, the configuration can be saved by simple saving the current configuration by selecting "Save As Script" from the "File" drop-down menu. This will save ALL the register status information. Once the file has been saved, it can be edited so that only the registers you are interested in changing are contained in the file. The "Save As Script" function will save everything including all the read only registers.

Scripts can be used to set up any static state you wish, but are limited to just setting the registers. There is not a provision to do delays between the sequences of register settings. You cannot, for instance, pulse dial with a script. Usually this should not be a significant limitation since normally only one static configuration is used at a time. To load a saved configuration, select the button under the Reset radio button or Load Script from the File menu and select the file that you want to load.

The CD contains sample scripts that can be used to quickly configure the board for specific purposes. This is a listing of the "setup-wg-init\_ofh.tsf" file. Everything necessary for operation is included in this script.

```
' 73M1966B Test Script File - setup-wg-init _ofh.tsf
' This script initializes the the 1966 registers
' after a hardware reset. It selects time slot 0
' operation. Make sure hardware reset is performed
' first! The 1966 will go off hook when executed.
' Script Format (All Values in Hex)
' Write Register: W, Mode, BRCT, CID, Address, Data
' Read Register: R, Mode, CID, Address, Data
                  Mode: 0=8-Bit, 1=16-Bit
                  BRCT: Only used in Write
                  CID, Address, Data: Hex Value
      GPI05-7 inputs set high
W,1,0,0,3,E0
      GPI05-7 =receivers
W,1,0,0,4,E4
      Enable detectors, polling ID
W,1,0,0,5,1B
      Enable line side device
W,1,0,0,F,80
      Enable OFH, DC, AC, FE, ENNOM
W,1,0,0,12,E5
      Set DCIV=10
W,1,0,0,13,80
      Set DAA=01, RXG=10
W,1,0,0,14,22
      Enable THEN
W,1,0,0,15,08
      Enable TXEN, RXEN, ATEN
W,1,0,0,16,D0
      Set DX polarity, timeslot 0
W,1,0,0,20,9F
      Set DR polarity, timeslot 0
W,1,0,0,21,1F
      Set clock slot for timeslot 0
W,1,0,0,22,3F
      Enable PCM
W,1,0,0,23,80
```

This is a listing of the "ring-rev-set-up.tsf" file:

```
Script - ring-rev-set-up (ON hook)
' This script is used to enable the ring/line reversal
 detection or to go ON hook, no CID
' The time slot is not affected and will remain as
 previously programmed
 Script Format (All Values in Hex)
 Write Register: W, Mode, BRCT, CID, Address, Data
      Write: W, Read: R
      Mode: 0=8-Bit, 1=16-Bit
      BRCT: Broadcast only used in Write
      Chip ID, Address, Data: Hex Value
      Enable detectors, polling ID bits
W,1,0,0,5,13
      Set ring signal threshold to 15V
W,1,0,0,E,01
      Enable barrier interface
W,1,0,0,F,80
      Enable line side device analog ckts
W,1,0,0,12,04
      All off hook functions disabled
W,1,0,0,15,00
      All off hook functions disabled
W,1,0,0,16,00
```

Note that the time slot is not being programmed in this case. This still would need to be done at some point, but it is not necessary to have a time slot selected if the PCM data is not being sent and received. There may also be cases where a specific time slot is being used other than time slot 0, so it would not be desirable to change to time slot zero every time the 73M1966B has a software reset.

In the following program example Caller ID can be received so the PCM receive channel must be configured. If the time slot is not programmed it will not be possible to receive the PCM data when the Caller ID signal is sent. It is not, however, necessary to program the PCMEN bit in register 23h since that is only required to send PCM. The receive analog channel must be turned on for the Caller ID path to be available, so the RXEN bit in register 16h must also be turned on. It was not really necessary to program the transmit channel time slot at this time, but it was done anyway so it won't need to be done separately later.

```
Script - ring-rev-CID-set-up (ON hook)
' This script is used to enable the ring/line reversal
' detection and Caller ID reception
' Script Format (All Values in Hex)
 Write Register: W, Mode, BRCT, CID, Address, Data
      Write: W, Read: R
      Mode: 0=8-Bit, 1=16-Bit
      BRCT: Broadcast only used in Write
      Chip ID, Address, Data: Hex Value
      Enable detectors, polling ID bits
W,1,0,0,5,13
      Set ring signal threshold to 15V
W,1,0,0,E,01
      Enable barrier device interface
W,1,0,0,F,80
      Enable
              line side device analog ckts
W,1,0,0,12,04
      20dB boost on for CID
W,1,0,0,14,08
      All off hook functions disabled; CID enabled
W,1,0,0,15,30
```

```
' Disable off hook functions except RXEN for CID
W,1,0,0,16,40
' Set DX polarity, timeslot 0 of WG
W,1,0,0,20,9F
' Set DR polarity, timeslot 0 of WG
W,1,0,0,21,1F
' Set clock slot for timeslot 0 of WG
W,1,0,0,22,3F
```

# 4 Related Documentation

The following 73M1x66B documents are available from Teridian Semiconductor Corporation:

73M1866B/73M1966B Data Sheet 73M1966B Evaluation Kit User Manual 73M1866/73M1966B Demo Board User Manual 73M1866/73M1966B Keychain Demo Board User Manual 73M1966 Layout Guidelines 73M1x66B Worldwide Design Guide

## **5** Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73M1866B or 73M1966B, contact us at:

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#### **Revision History**

Date	Description			
1/25/2008	First publication.			
3/23/2009	Re-wrote Section 3, Scripts.			
	Date 1/25/2008 3/23/2009			