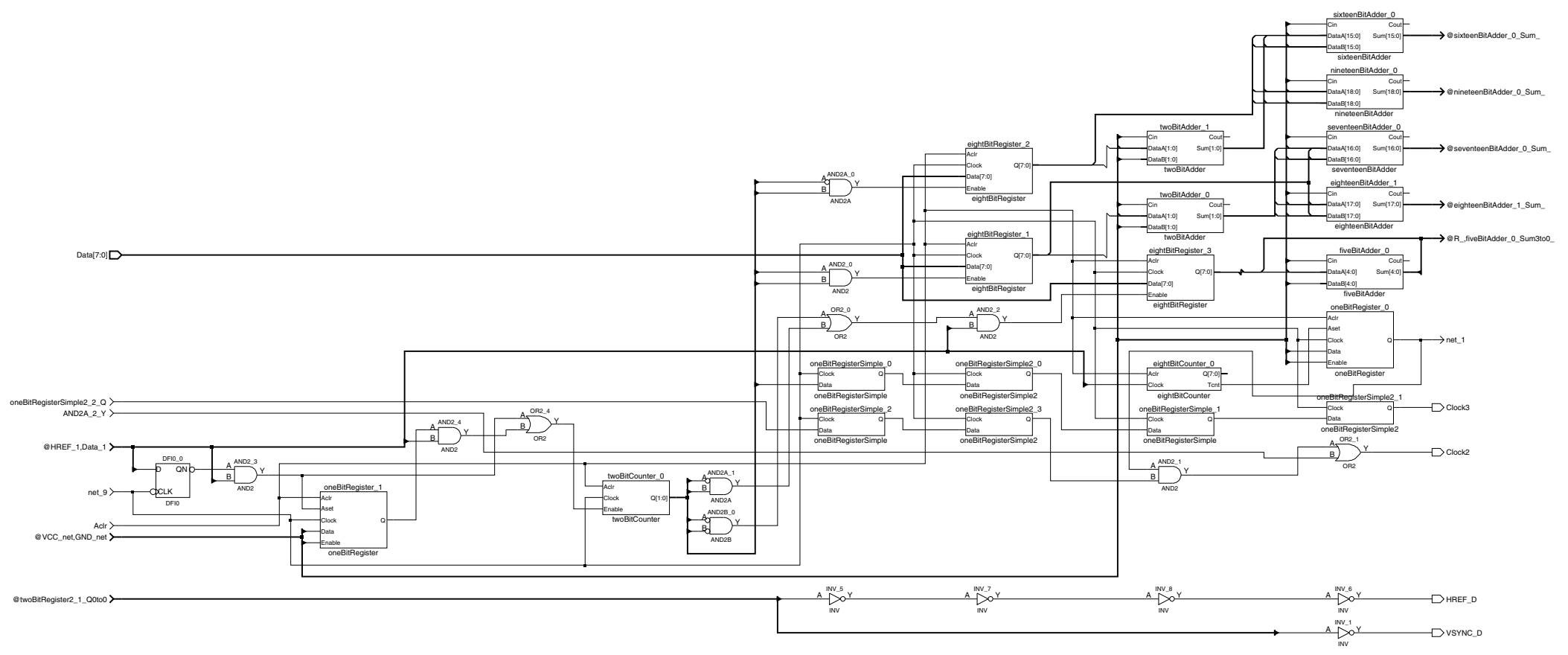
sixteenBitAdder_0
Cin
Cout
DataA[15:0]
Sum[15:0]
DataB[15:0]
sixteenBitAdder
@sixteenBitAdder_0_Sum_
nineteenBitAdder_0
Cin
Cout
DataA[18:0]
Sum[18:0]
DataB[18:0]
nineteenBitAdder
@nineteenBitAdder_0_Sum_
seventeenBitAdder_0
Cin
Cout
DataA[16:0]
Sum[16:0]
DataB[16:0]
seventeenBitAdder
@seventeenBitAdder_0_Sum_
eighteenBitAdder_1
Cin
Cout
DataA[17:0]
Sum[17:0]
DataB[17:0]
eighteenBitAdder
@eighteenBitAdder_1_Sum_
@R_.fiveBitAdder_0_Sum3to0_
fiveBitAdder_0
Cin
Cout
DataA[4:0]
Sum[4:0]
DataB[4:0]
fiveBitAdder
twoBitAdder_1
Cin
Cout
DataA[1:0]
Sum[1:0]
DataB[1:0]
twoBitAdder
twoBitAdder_0
Cin
Cout
DataA[1:0]
Sum[1:0]
DataB[1:0]
twoBitAdder
eightBitRegister_2
Aclr
Clock
Data[7:0]
Enable
Q[7:0]
eightBitRegister
eightBitRegister_1
Aclr
Clock
Data[7:0]
Enable
Q[7:0]
eightBitRegister
eightBitRegister_3
Aclr
Clock
Data[7:0]
Enable
Q[7:0]
eightBitRegister
AND2A_0
A
B
Y
AND2A
AND2_0
A
B
Y
AND2
OR2_0
A
B
Y
OR2
AND2_2
A
B
Y
AND2
Data[7:0]
oneBitRegister_0
Aclr
Aset
Clock
Data
Enable
Q
oneBitRegister
net_1
oneBitRegisterSimple_0
Clock
Data
Q
oneBitRegisterSimple
oneBitRegisterSimple_2
Clock
Data
Q
oneBitRegisterSimple
oneBitRegisterSimple2_0
Clock
Data
Q
oneBitRegisterSimple2
oneBitRegisterSimple2_3
Clock
Data
Q
oneBitRegisterSimple2
eightBitCounter_0
Aclr
Clock
Q[7:0]
Tcnt
eightBitCounter
oneBitRegisterSimple_1
Clock
Data
Q
oneBitRegisterSimple
oneBitRegisterSimple2_1
Clock
Data
Q
oneBitRegisterSimple2
Clock3
OR2_1
A
B
Y
OR2
Clock2
AND2_1
A
B
Y
AND2
oneBitRegisterSimple2_2_Q
AND2A_2_Y
@HREF_1,Data_1
net_9
Aclr
@VCC_net,GND_net
DFI0_0
D
QN
CLK
DFI0
AND2_3
A
B
Y
AND2
AND2_4
A
B
Y
AND2
OR2_4
A
B
Y
OR2
oneBitRegister_1
Aclr
Aset
Clock
Data
Enable
Q
oneBitRegister
twoBitCounter_0
Aclr
Clock
Enable
Q[1:0]
twoBitCounter
AND2A_1
A
B
Y
AND2A
AND2B_0
A
B
Y
AND2B
@twoBitRegister2_1_Q0to0
INV_5
A
Y
INV
INV_7
A
Y
INV
INV_8
A
Y
INV
INV_6
A
Y
INV
HREF_D
INV_1
A
Y
INV
VSYNC_D